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- Settings: 9600 baud, N, 8, 1
- Auto configuration supports 1200 through 9600 baud MODEMs

October 1993
Order Number: 297389-001

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Communication/Interface Controllers	
231928-001	AP-401 Designing with the 82510 Asynchronous Serial Controller
292038-001	AP-310 High Performance Driver for 82510
611001-001	AP-36 Using the 8273 SDLC/HDLC Protocol Controller
210311-002	AP-134 Asynchronous Communication with the 8274 Multiple-Protocol Serial Controller
210403-001	AP-145 Synchronous Communication with the 8274 Multiple Protocol Serial Controller
231262-004	AP-222 Asynchronous and SDLC Communications with 82530
230832-001	AP-166 Using the 8291A GPIB Talker/Listener
231324-002	AP-66 Using the 8292 GPIB Controller

Modem Products

1

89024
2400 BPS INTELLIGENT MODEM CHIP SET

- For Public Switched Telephone Network and Unconditioned Leased Line Applications
- V.22 bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- AT Command Set
- Automatically Adapts to Remote Modem Type with Recognition of Data Rates
- DTMF and Pulse Dialing
- On-Chip Hybrid and Billing Delay Timer
- On-Chip Serial Port and Handshake Signals for RS-232/V.24 Interface
- Telephone Line Audio Monitor Output
- Analog/Digital Loopback Diagnostics
- Serial Interface to External NVRAM
- Easily Customized Command Set and Features
- Two Chip Intelligent Modem Solution with Minimal External Components
- Output Level Programmable over 16 dB Range
- Dial and Re-dial Capability
- Full Set of Control Signals for DAA Interface
- Local, External, or Slave Timing Options in Synchronous Mode
- Adaptive Equalization
- Capable of Detecting Dial, Busy, Ringback and Modem Answer Tones of Most International Networks
- Auxiliary Relay Control Output
- Packaging:
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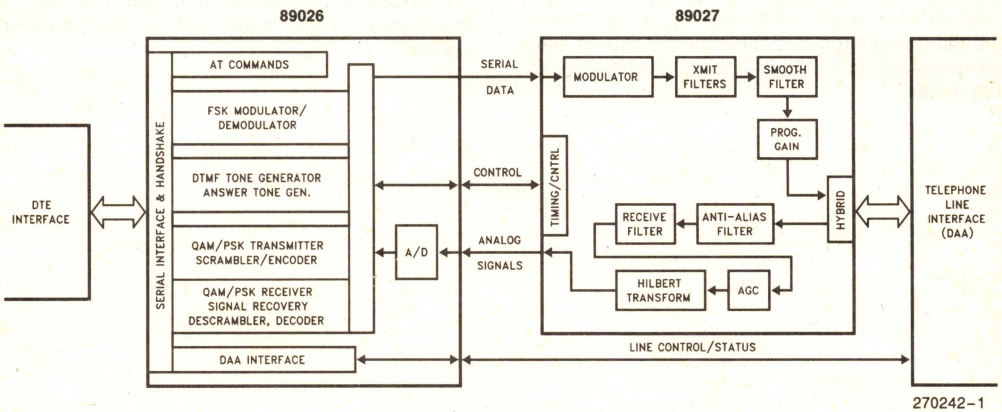


Figure 1. 89024 System Block Diagram

November 1991
Order Number: 270242-006

GENERAL DESCRIPTION

The Intel 89024 chip set is a highly integrated, high performance, intelligent modem, providing a complete system in two chips. The system is compatible with the following CCITT and Bell standards:

- CCITT V.22 bis
  2400 bps sync and async
  1200 bps sync and async (fall-back)
- CCITT V.22 A & B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous

The 89024 system consists of a 16 bit application specific processor (89026) and an analog front end device (89027). The 89026 processor performs all "Digital Signal Processing" algorithm execution for processing the modem signals, as well as providing all modem control functions typically performed by an external processor. The analog front end provides for 2 wire and 4 wire telephone line interface, D/A conversion, and most of the complex filtering functions required in QAM/PSK/FSK modems. Refer to Figure 1 for a simplified block diagram of the system.

In stand-alone modem applications, the 89024 chip set along with a Data Access Arrangement (DAA), a serial NVRAM, and RS-232 driver/receivers, represent the circuitry required for implementing an auto-dial, auto-answer, 300 to 2400 bps, full duplex intelligent modem.

A complete set of industry standard AT commands is provided for modem configuration and user interface. Virtually all PC software written for the AT command set can also be used with this chip set. Alternatively, in applications where user proprietary modem control commands and features are desired, the user can replace the 89024 internal command module with custom proprietary software resident in the 89026 microcontroller's on-chip ROM or an external memory device.

The 89024 supports two versions of firmware. These are internal, which is asynchronous only and external, which is asynchronous and synchronous. Any differences in operation are highlighted with footnotes.

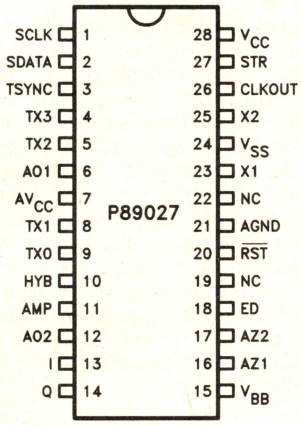
The 89024 has a set of default features. Upon power up, the modem configuration will be in accordance with these default options, unless a different configuration has been saved in the external NVRAM with the &W command.

The 89024 modem has built in auto-dialing and auto-answering capabilities. It can be configured to the proper line signaling mode (Tone or Pulse), and to to the type (CCITT or Bell) and speed of the calling or answering modem. It can also detect and identify call set-up signals of telephone networks, allowing unattended data call operation.

A full set of diagnostic loop-test features compatible with CCITT V.54 is supported. The chip set also provides a line signal for audio monitoring of call progress, a comprehensive set of DAA control lines for a simple interface to the telephone network, and a full complement of TTL level RS-232/ V.24 handshake signals.

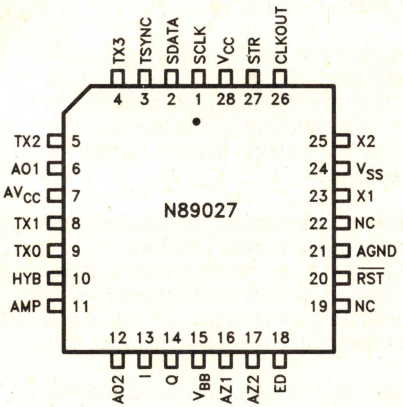
PACKAGING

The 89027 is available in PLCC and standard plastic DIP packages. The 89026 is available in a PLCC package.



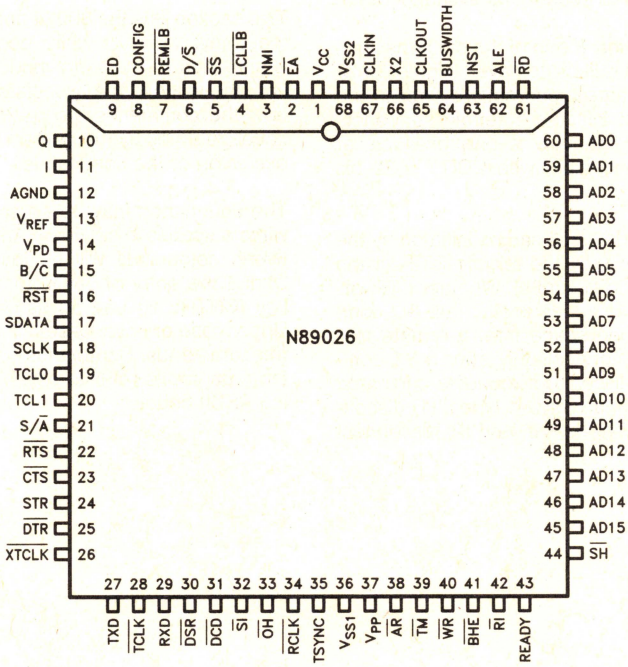
270242-2

28 Pin Plastic DIP



270242-3

28 Pin PLCC



270242-5

68 Pin PLCC

Figure 2. Device Packages

CALL ESTABLISHMENT, TERMINATION AND RETRAIN

The 89024 modem system incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The modem chip-set has a built-in auto-dialer, both DTMF and Pulse type. The modem can detect the dial, busy, and ringback signals at remote end, and will provide call progress messages to the user. The modem is capable of re-dialing the last number dialed, by one command.

The modem when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, before transmitting the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be setup by manual dialing with the modems set to data mode, or by voice to data transfer by means of mechanical switch (exclusion key), using the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22 bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE, (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect, depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests originated by the remote modem, are of two types, (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip-set can also be configured to transmit 'long-space' just before disconnection, in each of the aforementioned cases.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22 bis to 212A), the Intel chip-set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22 bis standard, transparently, to 212A users. Similarly, a user with a 89024 based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89024 commands and registers that may be used while configuring the modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered in a string, with or without spaces in between. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the 'backspace' key (CNTRL H) can be used to correct any error. Upper case or lower case characters can be used in the commands. Commands described in the following paragraphs refer to asynchronous terminals using ASCII codes.

Table 1. Remote Modem Compatibility

Originating 89024 Modem		Answering Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89024 Modem		Originating Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

* These connection data rates are obtained when connecting 89024 based modems end to end. The same results may not be obtained when a 89024 based modem is connected to other modems.

Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn(1)	BELL/CCITT Protocol Compatibility at 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ; @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code

& Command Set

&C	DCD Options
&D	DTR Options
&F	Fetch Factory Configuration Profile
&G	Guard Tone
&J	Telephone Jack Selection
&L	Leased/Dial-up Line Selection
&M(1)	Async/Sync Mode Selection
&P	Make/Break Pulse Ratio
&R	RTS/CTS Options
&S	DSR Options
&T	Test Commands
&W	Write Configuration to Non Volatile Memory
&X(1)	Sync Clock Source
&Z	Store Telephone Number

NOTE:
1. Available in external code only.

CONFIGURATION REGISTERS

The modem stores all the configuration information in a set of registers. Some registers are dedicated to special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11**	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register

NOTE:
* These S registers can be stored in the NVRAM.
**Available in internal code only.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z T 1 (602) 555-1212
Modem: OK

Result: Modem stores T16025551212 in the external NVRAM.

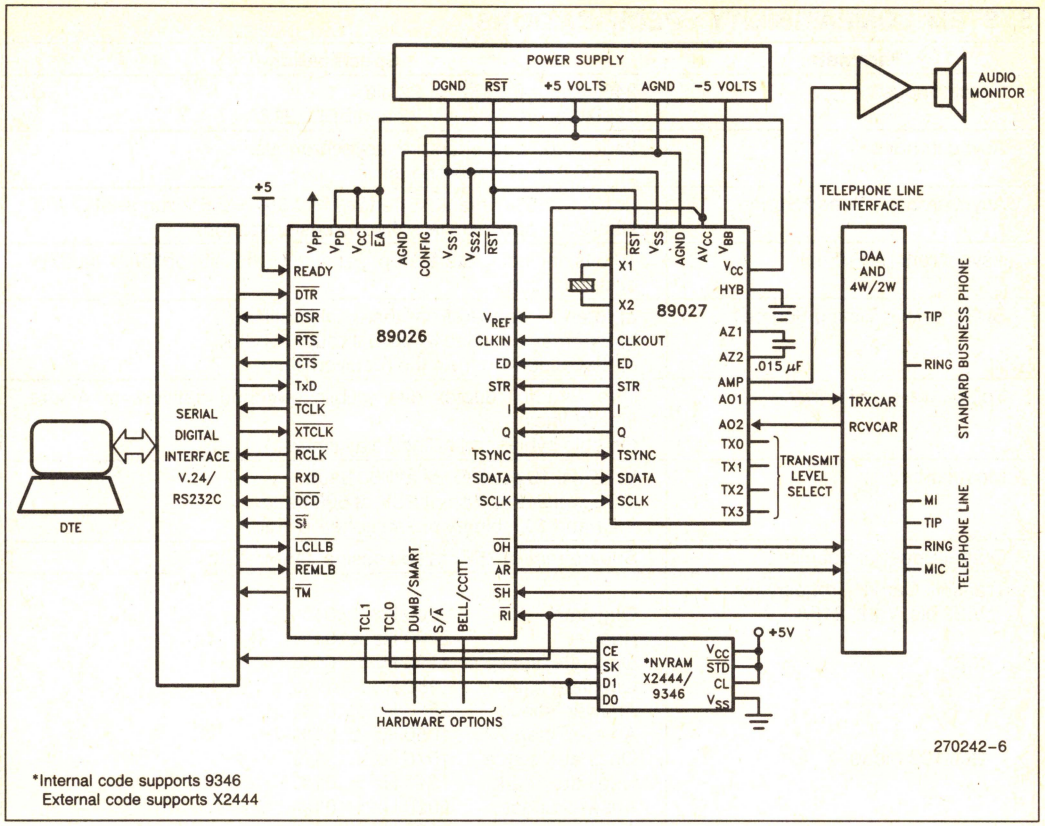
The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS
Modem: T16025551212

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 3. The DAA section shown in this diagram may be obtained with FCC registration, or implemented using the suggested diagram in Figure 4.



*Internal code supports 9346
External code supports X2444

Figure 3. Typical Modem Configuration with External Hybrid

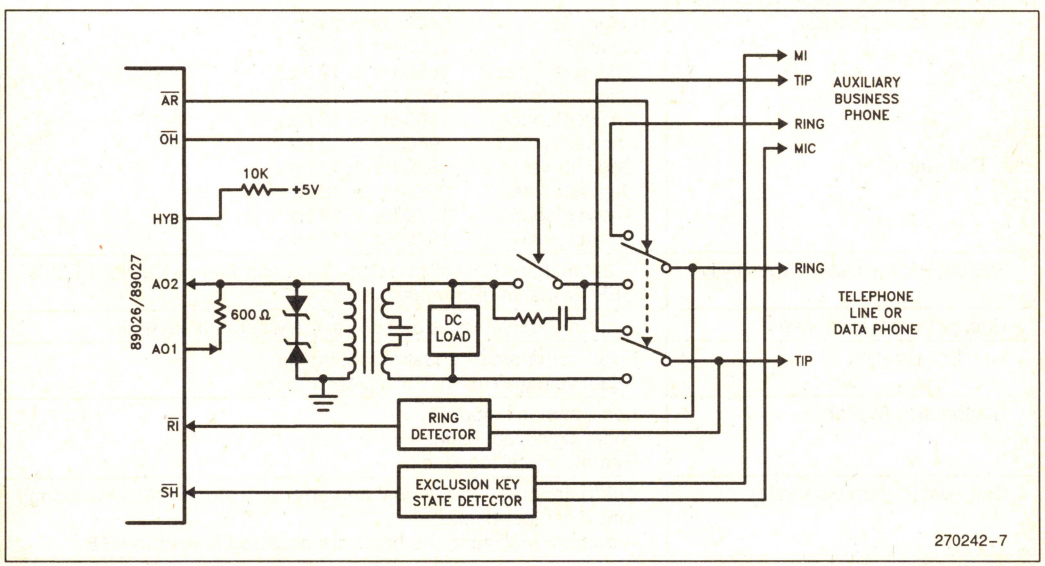


Figure 4. Typical Telephone Line Interface Using Internal Hybrid

SYSTEM COMPATIBILITY SPECIFICATIONS

Parameter	Specification
Synchronous*	2400 bps ±0.01% V.22 bis 1200 bps ±0.01% V.22 and BELL 212A
Asynchronous	2400, 1200 bps, character asynchronous. 0 - 300 bps anisochronous.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. 8, 9, 11 bits optional via S/W customization.
Synchronous Timing Source*	a) Internal, derived from the local oscillator. b) External, provided by DTE through $\overline{\text{XTCLK}}$. c) Slave, derived from the received clock.
Telephone Line Interface	Two wire full duplex over public switched network or 4 wire leased lines. On-chip hybrid and billing delay timers.
Modulation	V.22 bis, 16 point QAM at 600 baud. V.22 and 212A, 4 point PSK at 600 baud. V.21 and 103, binary phase coherent FSK
Output Spectral Shaping	Square root of 75% raised cosine, QAM/PSK.
Transmit Carrier Frequencies V.22 bis, V.22, 212A V.21 Bell 103 mode	 Originate 1200 Hz ± .01% Answer 2400 Hz ± .01% Originate 'space' 1180 Hz ± .01% Originate 'mark' 980 Hz ± .01% Answer 'space' 1850 Hz ± .01% Answer 'mark' 1650 Hz ± .01% Originate 'space' 1070 Hz ± .01% Originate 'mark' 1270 Hz ± .01% Answer 'space' 2020 Hz ± .01% Answer 'mark' 2225 Hz ± .01%
Receive Carrier Frequency Limits V.22 bis, V.22, 212A V.21 Bell 103	 Originate 2400 Hz ± 7 Hz Answer 1200 Hz ± 7 Hz Originate 'space' 1850 Hz ± 12 Hz Originate 'mark' 1650 Hz ± 12 Hz Answer 'space' 1180 Hz ± 12 Hz Answer 'mark' 980 Hz ± 12 Hz Originate 'space' 2020 Hz ± 12 Hz Originate 'mark' 2225 Hz ± 12 Hz Answer 'space' 1070 Hz ± 12 Hz Answer 'mark' 1270 Hz ± 12 Hz
Typical Energy Detect Sensitivity	Greater than −43 dBm ED is ON. Less than −48 dBm ED is OFF. Signal in dBm measured at A02.
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.
Line Equalization	Fixed compromise equalization, transmit. Adaptive equalizer for PSK/QAM, receive.
Diagnostics Available	Local analog loopback. Local digital loopback. Remote digital loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeros' and error detector, to be used along with most loopbacks. A number indicating the bit errors detected is sent to DTE.

*External code only.

RECEIVER PERFORMANCE

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	**Rx Level (dBm)**	**Answer (dB)**	**Originate (dB)**
V.22 bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

—Recieve signal (Rx) measured at A02 (transmit level set at −9 dBm)

—Unconditioned 3002 line

—3 kHz Flat-band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10		pps	
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	 referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89026 OVERVIEW

The 89026 processor performs data manipulation, signal processing and user interface functions. It supports an external ROM, for user designed software. This option allows customer designed code to control the signal processing algorithms resident in the 89026. For example proprietary modem control and call progress management applications can be implemented using EPROMs or alternatively by having it burnt in the processor ROM (done so by Intel factory contracting). On-chip ROM is 8 Kbytes. A block diagram of 89026 is in Figure 5.

89026 contains a TTL compatible serial link to DTE/DCE equipment, along with a full complement of V.24/RS-232-C control signals. Alternatively, UART or USART may be used to directly transfer data to and from a microcomputer bus. The 89024 supports the industry standard AT command set, facilitating compatibility with most PC software.

In the transmit operation, the 89026 synthesizes DTMF tones and the 300 bps FSK modem signal prior to transmitting them to the 89027 as digitized amplitude samples. During 1200 and 2400 bps operation, PSK and QAM is used to send 2 or 4 bits of information respectively at 600 baud to 89027. Since the QAM coding technique is an inherently synchronous transmission mechanism, during asynchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89026 transmits digitized phase and amplitude samples to 89027 over a high speed serial link.

In the receive operation, the information is received by 89026 from 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the 89026's onboard A/D converter, and using DSP software algorithms the signals are gain adjusted, adaptively equalized for telephone line delay and amplitude distortion, and demodulated. Following the demodulation process by the 89026, the data is unscrambled, and if necessary, returned to asynchronous format.

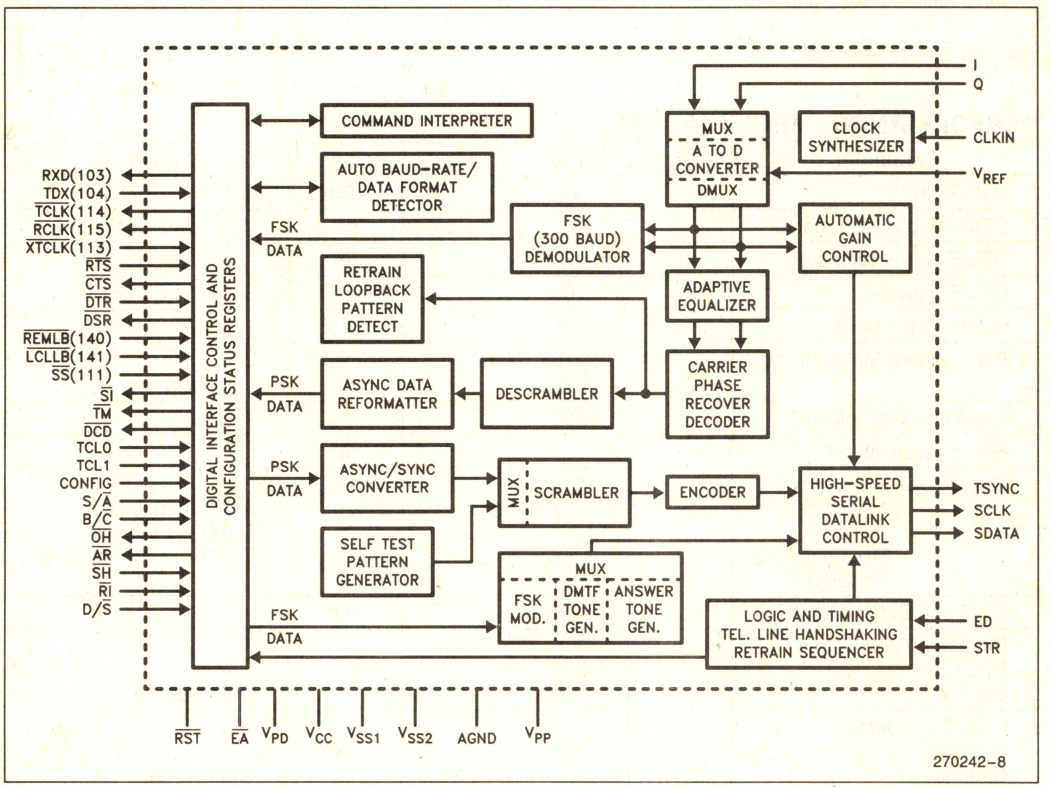


Figure 5. 89026 Block Diagram

89026 PINOUT

Symbol	Function (89026)	Direction	Pin No.
			68 pin
CLKIN	12.96 MHz master clock from 89027	In	67
$\overline{RST}$	Chip reset (active low)	In	16
I	In-phase received signal	In	11
Q	Quadrature-phase received signal	In	10
STR	Symbol Timing from 89027	In	24
ED	Energy Detect input	In	9
TSYNC	Transmitter sync pulse to 89027	Out	35
SDATA	Serial Data to 89027	Out	17
SCLK	Serial Clock to 89027	Out	18
$\overline{OH}$	Off-Hook control to DAA	Out	33
$\overline{SH}$*	Switch-Hook from dataphone	In	44
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay control to DAA	Out	38
TCL1	NVRAM Data I/O	I/O	20
TCL0	NVRAM CLK	Out	19
B/$\overline{C}$*	103/V.21 default option	In	15
S/$\overline{A}$	NVRAM $\overline{CE}$	Out	21
D/$\overline{S}$	Dumb/$\overline{Smart}$ mode select	In	6
CONFIG	Reserved for future use (V_{CC})(3)	In	8
$\overline{TM}$	Test Mode Indicator	Out	39
TXD	Transmitted data from DTE	In	27
RXD	Received data to DTE	Out	29
$\overline{RTS}$	Request to send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received clock to DTE	Out	34
$\overline{TCLK}$	Transmit clock to DTE	Out	28
$\overline{XTCLK}$*	External timing clock from DTE	In	26
$\overline{SI}$	Speed Indicator to DTE	Out	32
$\overline{SS}$	(Note 4)	In	5
$\overline{REMLB}$*	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$*	Local Loopback Command from DTE	In	4
V_{CC}	Positive power supply (+5V)	+5V	1
V_{PD}	Ram back-up power (V_{CC})(3)	+5V	14
V_{REF}	A/D converter reference	+5V	13
V_{SS1}	Digital ground	GND	36
V_{SS2}	Digital ground	GND	68
AGND	Analog ground	AGND	12
V_{PP}	(NC)(2)	In	37
$\overline{EA}$	External Memory enable	In	2
AD0-AD15	External memory access address/data(5)	I/O	60-45
$\overline{AA}$	Auto Answer(5)	Out	60
$\overline{JS}$	Jack Select(5)	Out	59
$\overline{CD}$	Carrier Detect Indicator(5)	Out	58
$\overline{MR}$	Modem READY Indicator(5)	Out	57

*Available in external code only.

89026 PINOUT (Continued)

Symbol	Function (89026)	Direction	Pin No.
			68 pin
NMI	No-maskable Interrupt(V_{SS})(1)	In	3
X2	Crystal output(NC)(2)	Out	66
CLKOUT	Clk output (NC)(2)	Out	65
BUSWIDTH	Bus Width (V_{CC})(3)	In	64
INST	External memory instruction fetch	Out	63
ALE	Address latch enable	Out	62
$\overline{RD}$	External memory read	Out	61
READY	External memory ready(V_{CC})(3)	In	43
$\overline{BHE}$	External memory bus high enable	Out	41
$\overline{WR}$	External memory write	Out	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (NC) are to be left unconnected.
3. Pins marked with (V_{CC}) must be connected to V_{CC}.
4. $\overline{SS}$ pin reserved for future use.
5. With internal ROM enabled, AD0–AD3 are used as $\overline{AA}$, $\overline{JS}$, $\overline{CD}$ and $\overline{MR}$ respectively.
6. Pins with direction "In" must not be left floating.

89026 PIN DESCRIPTION

$\overline{XTCLK}$*

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89026 samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$*

Clock output from 89026 as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. 'Mark' is a logic High. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$*

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

V_{PP}

This function is not used and should not be connected.

$\overline{TM}$

A Low indicates maintenance condition in the modem.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains Low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation Low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

Low indicates modem is off-hook, and it is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ Low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a Low to High transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A Low to High transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

B/$\overline{C}$*

Low configures the modem to CCITT V.21. High will configure the modem to Bell 103, when at 300 bps speed. This pin only affects the modem in FSK operation.

*External code only.

TCL1, TCL0

These pins are used as the serial clock and data for interface to an NVRAM. Refer to Figure 3. TCL0 is used to output a clock and serial data is transferred on TCL1.

$\overline{AR}$

This Auxiliary relay control is for switching a relay for voice or data calls. High is voice, Low is data.

$\overline{RI}$

A Low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high sets an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$*

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state. This input is ignored, if a software command attempts to switch the modem between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$*

A Low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins, sets the modem to the local digital loopback.

$\overline{REMLB}$*

A logic Low on this pin initiates a remote loopback condition.

*External code only

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 BELL) or range of rates. High selects the Low rate or range of rates.

D/$\overline{S}$

A Low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89027 AVcc.

V_{PD}

The internal RAM power down supply voltage to be connected to 5 Volts during normal operation.

S/$\overline{A}$

The function of this pin is re-defined as external NVRAM CE.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When High, memory access from address 2000H to 4000H are directed to on-chip ROM. When Low, all memory access is directed to off-chip memory.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

$\overline{CD}$

A low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test move is active.

89026 ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias ..... 0°C to +70°C

Storage Temperature ..... −40°C to +125°C

Voltage from Any Pin to V_{SS} or AGND ..... −0.3V to +7.0V

Average Output Current from Any Pin ..... 10 mA

Power Dissipation ..... 1.5 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
TA	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
FREQ	CLKIN Frequency 12.96 MHz	−0.01%	+0.01%	
V_{PD}	Power-Down Supply Voltage	4.75	5.25	V

NOTE:
The AGND and V_{SS} on both the 89026 and the 89027 must be nominally at the same potential.

D.C. CHARACTERISTICS

Test Conditions: V_{CC}, V_{REF}, V_{PD}, V_{PP}, V_{EA} = 5.0V ±0.25V; F_{OSC} = 12.96 MHz; T_A = 0°C to 70°C, V_{SS}, AGND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current (0°C ≤ T_A ≤ 70°C)		240	mA	All Outputs Disconnected
I_{CC1}	V_{CC} Supply Current (T_A = 70°C)		185	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal Operation and Power-Down
I_{REF}	V_{REF} Supply Current		8	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, CLKIN)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling Hysteresis	2.1	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage, NMI, CLKIN	2.2	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current(1)		±10	μA	V_{IN} = 0 to V_{CC}
I_{LI1}	D.C. Input Leakage Current(2)		+3	μA	V_{IN} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current(3)		−125	μA	V_{IL} = 0.45V
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current, READY, BUSWIDTH(4)		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage(5)		0.45	V	I_{OL} = 0.8 mA
V_{OL1}	Output Low Voltage(5)		0.75	V	I_{OL} = 2.0 mA
V_{OL2}	Output Low Voltage(6) $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage(5)	2.4		V	I_{OH} = −20 μA
V_{OH1}	Output High Voltage on Bus Control Pins(7)	2.4		V	I_{OH} = −200 μA
I_{OH3}	Output High Current on $\overline{RESET}$	−50		μA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	f_{TEST} = 1.0 MHz

NOTES:
1. STR, $\overline{DTR}$, $\overline{XTCLK}$, TXD
2. S/$\overline{D}$, $\overline{SS}$, $\overline{REMLB}$, $\overline{LCLLB}$, I, Q, CONFIG, ED
3. $\overline{TCLK1}$, $\overline{RTS}$
4. Also, B/$\overline{C}$, $\overline{SH}$, $\overline{RI}$
5. TCL0, S/$\overline{A}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, SI, $\overline{OH}$, $\overline{AR}$
6. SCLK, SDATA, $\overline{TM}$, $\overline{TCLK}$, RXD, $\overline{RCLK}$, TSYNC
7. Bus/Control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.

AC CHARACTERISTICS (V_{CC}, V_{PD} = 4.75 to 5.25 Volts; T_A = 0°C to 70°C; CLKIN = 12.96 MHz)

Test Conditions: Load capacitance on output pins = 80 pF
T_{OSC} = 1/12.96 MHz

TIMING REQUIREMENTS (Other system components must meet these specs.)

Symbol	Parameter	Min	Max	Units
T_{CLYX}	READY Hold after CLKOUT Edge	0		ns
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		2Tosc − 70	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	2Tosc +40	4Tosc − 80	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(1)	Address Valid to Input Data Valid		5Tosc − 120	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		3Tosc − 100	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	Tosc − 25	ns
T_{AVGV}(1)	Address Valid to BUSWIDTH Valid		2Tosc − 125	ns
T_{LLGX}	BUSWIDTH Hold after ALE/$\overline{ADV}$ Low	Tosc + 40		ns
T_{LLGV}	ALE/$\overline{ADV}$ Low to BUSWIDTH Valid		Tosc − 75	ns

NOTE:
1. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.

TIMING RESPONSES

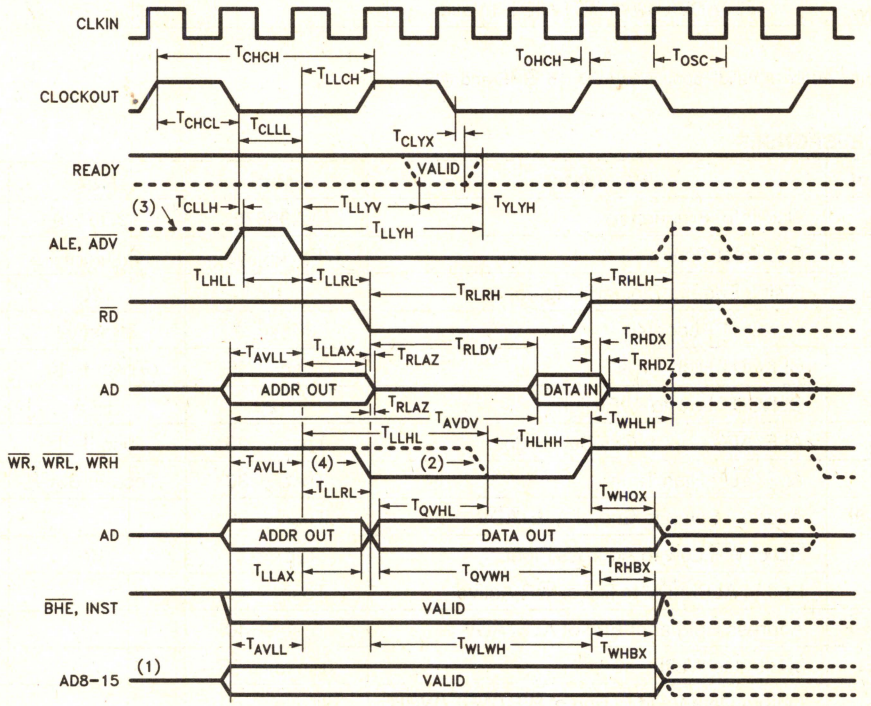
Symbol	Parameter	Min	Max	Units
F_{CLKIN}	Oscillator Frequency	12.95870	12.96129	MHz
T_{OSC}	Oscillator Period	1/$F_{CLKIN(MAX)}$	1/$F_{CLKIN(MIN)}$	ns
T_{OHCH}	Rising Edge to Clock Rising Edge	0	120	ns
T_{CHCH}	CLKOUT Period(2)	3Tosc(2)	3Tosc(2)	ns
T_{CHCL}	CLKOUT High Time	Tosc − 35	Tosc + 10	ns
T_{CLLH}	CLKOUT Low to ALE High	−20	+25	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	Tosc − 25	Tosc + 45	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	Tosc − 30	Tosc + 35(3)	ns
T_{AVLL}(4)	Address Setup to End of ALE/$\overline{ADV}$	Tosc − 50		ns
T_{RLAZ}	$\overline{RD}$ or $\overline{WR}$ Low to Address Float	Typ. = 0	10	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active	Tosc − 40		ns
T_{LLAX}(5)	Address Hold after End of ALE/$\overline{ADV}$	Tosc − 40		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	3Tosc − 35		ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	3Tosc − 60		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	Tosc − 50		ns
T_{WHLH}	End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ High	Tosc − 75		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	3Tosc − 30		ns
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	Tosc − 45		ns

TIMING RESPONSES (Continued)

Symbol	Parameter	Min	Max	Units
T_{CLLL}	CLKOUT to Low ALE/$\overline{ADV}$ Low	Tosc − 40	Tosc + 35	ns
T_{RHBX}	$\overline{RD}$ High to INST, $\overline{BHE}$, AD8–15 Inactive	Tosc − 25	Tosc + 30	ns
T_{WHBX}	$\overline{WR}$ High to INST, $\overline{BHE}$, AD8–15 Inactive	Tosc − 50	Tosc + 100	ns
T_{HLHH}	$\overline{WRL}$, $\overline{WRH}$ Low to $\overline{WRL}$, $\overline{WRH}$ High	2Tosc − 35	2Tosc + 40	ns
T_{LLHL}	ALE/$\overline{ADV}$ Low to $\overline{WRL}$, $\overline{WRH}$ Low	2Tosc − 30	2Tosc + 55	ns
T_{QVHL}	Output Data Valid to $\overline{WRL}$, $\overline{WRH}$ Low	Tosc − 60		ns

NOTES:
1. If more than one wait state is desired, add 3Tosc for each additional wait state.
2. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3Tosc ±10 ns if Tosc is constant and the rise and fall times are less than 10 ns.
3. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
4. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
5. The term "Address" in this definition applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.

WAVEFORM



NOTES:
1. 8-bit bus only
2. 8-bit or 16-bit bus and write strobe mode selected.
3. When $\overline{ADV}$ selected.
4. 8- or 16-bit bus and no write strobe mode selected.

Figure 6. Bus Signal Timings

89027 OVERVIEW

The 89027 is a 28 pin CHMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 7. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89027 functions are controlled by 89026, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89026. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through an on-board programmable gain amplifier.

During the receive operation, the received FSK and QAM signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89026 processor as analog signals.

Other functions provided by the 89027 are: an on-board two wire to four wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89027 is available in 28 pin plastic DIP and PLCC packages.

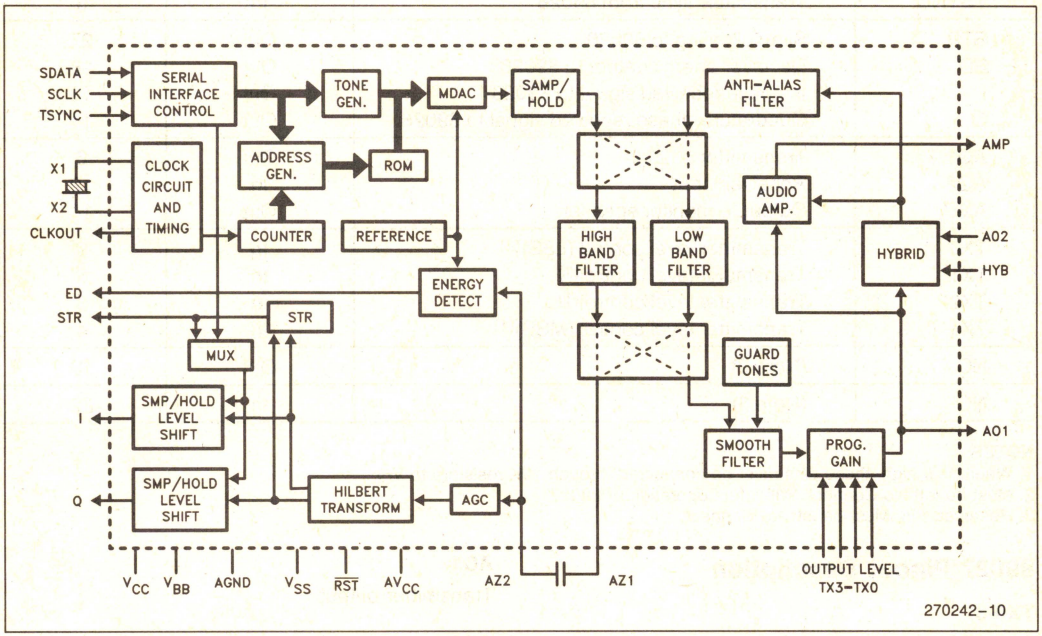


Figure 7. 89027 Block Diagram

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock Output to 89026	Out	26
$\overline{RST}$	Chip reset (active low)(1)	In	20
HYB	Enable on-chip hybrid(1)	In	10
AZ1	Auto-zero capacitor	Out	16
AZ2	Auto-zero capacitor	In	17
SDATA	Serial data from 89026	In	2
SCLK	Serial clock from 89026	In	1
TSYNC	Transmitter sync from 89026	In	3
STR	Symbol timing to 89026	Out	27
ED	Receiver energy detect to 89026	Out	18
I	In phase received signal to 89026	Out	13
Q	Quadrature-phase received signal to 89026	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control (LSB)(1)	In	9
TX1	Transmitter level control(1)	In	8
TX2	Transmitter level control(1)	In	5
TX3	Transmitter level control (MSB)(1)	In	4
NC	(Note 2)	Out	19
NC	(Note 3)	In	22

NOTES:
1. When held high, these pins must be connected through 10K resistors to V_{CC}.
2. Must be left No Connect. Will affect operation of 89027
3. Reserved Pin. Must be left No Connect.

89027 Pinout Description

TX0-3

These four pins control the transmitted signal level. Refer to Transmit Level Table.

HYB

This pin enables the on-chip hybrid. A line impedance matching network must be connected between AO1 and AO2 when HYB is enabled. If HYB is disabled and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AO1

Transmitter output.

AO2

Receiver input.

AMP

This output can be used to monitor the call progress tones and operation of the line.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −0 to +70°C

Storage Temperature..... −40 to +125°C

All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V

All Input and Output Voltages with Respect to V_{CC} & AV_{CC}..... −13.0V to 0.3V

Power Dissipation 1.35W

Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

NOTE:
1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0–TX3 only.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

POWER DISSIPATION Ambient Temp = 0°C to 70°C, V_{CC} = AV_{CC} = 5V ±5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$Aicc_1$	AV_{CC} Operating Current		15	21	mA
Icc_1	V_{CC} Operating Current		5	6	mA
Ibb_1	V_{BB} Operating Current		−15	−21	mA
Aiccs	AV_{CC} Standby Current		0.2	1	mA
Iccs	V_{CC} Standby Current		5	6	mA
Ibbs	V_{BB} Standby Current		−0.6	−2	mA
Pdo	Operating Power Dissipation		175	250	mW
Pds	Standby Power Dissipation		30	50	mW

DC CHARACTERISTICS (Ta = 0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89026 power supply. Typical Values are for Ta = 25°C and nominal power supply values. V_{CC}, AV_{CC} and 89026 V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: CLKOUT

Symbol	Parameter	Min	Max	Units	Test Condition
Iil	Input Leakage Current	−10	+10	µA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.4	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50µa, 1 TTL load
V_{col}	CLKOUT Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	CLKOUT High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

AC CHARACTERISTICS (T_a = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V < Vin < +2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20 %
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

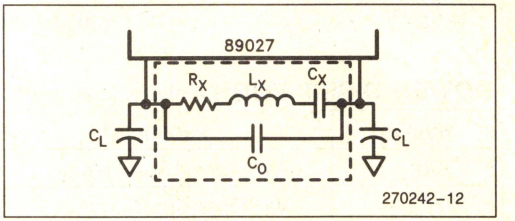


Figure 8. Crystal Equivalent Circuit

CRYSTAL REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Comments
Frequency Accuracy (0°C–70°C)	−0.0035%	12.96	+0.0035%	MHz	Refer to Figure 8
Rx		10	16	Ohms	
Cx		0.024		pF	
Co	5.1	5.6	6.1	pF	
C_L	−5%	33	+5%	pF	2 Load Capacitors

Crystal Type: Parallel Resonant

ANALOG OUTPUTS: AO1, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance					
AO1	600			Ohms	
AMP	10			KOhms	
Load Capacitance					
AMP			100	pF	
Audio Amp Gain AO1 to Amp		−9		dB	Max
		−18		dB	Mid
		−26		dB	Min Software
		−70		dB	Off Selectable
Audio Amp Gain (1) AO2 to Amp		+12		dB	Max
		+3		dB	Mid
		−4		dB	Min Software
		−60		dB	Off Selectable

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

TRANSMIT LEVEL

TRANSMIT OUTPUT LEVEL(1)		
TX 3,2,1,0	**Typ**	**Units**
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK, signal levels are typically 1 dB lower. All signals are measured at AO1.
2. The tolerance for the above transmit levels are ±1 dBm.

REFERENCE MANUALS

The *Modem Reference Manual* (Order Number 296235-002) contains pin descriptions, schematics, and important design guidelines for this chipset (89024) as well as for the 89C024LT and 89C024FT modem chip sets.

The *Modem Software Reference Manual* (Order Number 296503-001) provides information about the modem software routines. Contact your local sales office for the latest information.

89024 REVISION -006 HISTORY

The following differences exist between Rev. -005 and this version of the data sheet:

1. $\overline{CD}$ and $\overline{MR}$ signal indicator descriptions added.

89C024LT
ERROR CORRECTING LAPTOP MODEM CHIP SET

- CHMOS for Low Operating Power
- Low Standby Power Requirements
- Minimum Chip Count for Small size
- MNP* Operation through Class 4 for Error Correction
- MNP Class 5 Data Compression for Increased Throughput
- AT Command Set
- V.22 bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- For Public Switched Telephone Network and Unconditioned Leased Line Applications
- Automatically Detects Remote Modem Type and Data Rate
- On-Chip Hybrid
- DTMF and Pulse Dialing
- On-Chip Serial Port and Handshake Signals for RS-232/V.24 Interface
- Serial Interface to External NVRAM
- Automatic Speed Matching in MNP and Normal Modes
- Hardware and Software Flow Control
- Analog/Digital Loopback Diagnostics
- Telephone Line Audio Monitor Output
- Full Set of Control Signals for DAA Interface
- International Call Progress Tone Detection Capabilities
- Automatic Adaptive Equalization
- Synchronous Modes
- Easily Customized Command Set and Features
- Intel's MNP Software Co-Developed with R. Scott Associates**
- Packaging:
  - — For Packages
    QN89026LT SV782 68-Pin PLCC
    QN89027 28-Pin PDIP
    Order Kit #89C024LT SZ504
  - — For Packages
    QN89026LT SV782 68-Pin PLCC
    QN89027 28-Pin PLCC
    Order Kit #89C024LT SZ505

(See Packaging Specifications Order Number 240800-001)

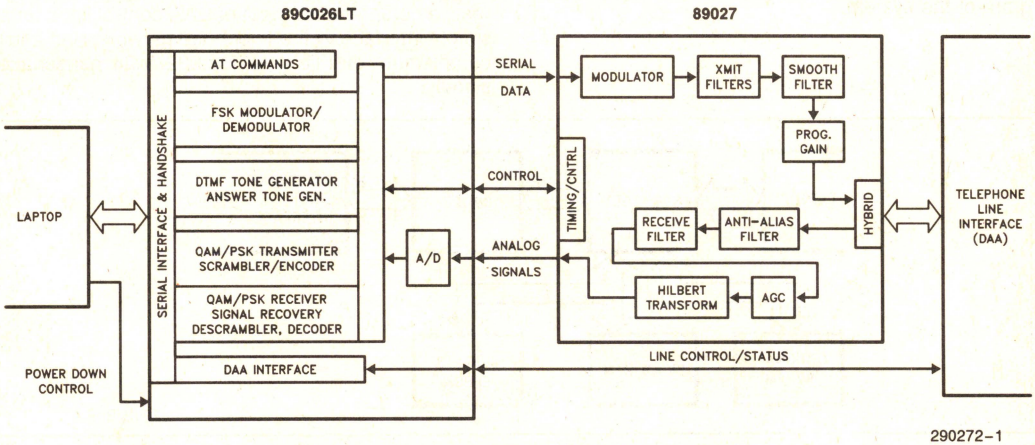


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Figure 1. 89C024LT System Block Diagram

*MNP is a registered trademark of Microcom, Inc.
**R. Scott Associates, Inc., 5711 Six Forks Road, Suite 301, Raleigh, North Carolina 27609, (919) 846-7171

October 1993
Order Number: 290272-005

GENERAL DESCRIPTION

Intel 89C024LT is a highly integrated, low power, error correcting laptop modem chip set. This two chip solution is composed of the 89027 Analog Front End and 89C026LT microcontroller. At 12.96 MHz the microcontroller is capable of executing error correction and data compression routines. The system is compatible with the following CCITT and BELL standards.

- CCITT V.22 bis
  2400 bps sync and async
  1200 bps sync and async
- CCITT V.22 A & B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous

The 89C024LT system consists of a 16 bit application specific processor (89C026LT) and an analog front end device (89027). The 89C026LT processor performs all "Digital Signal Processing" algorithm execution for processing the modem signals, as well as providing all modem control functions typically performed by an external processor. The analog front end provides for 2 wire and 4 wire telephone line interface, D/A conversion, and most of the complex filtering functions required in QAM/PSK/FSK modems. Refer to Figure 1 for a simplified block diagram of the system.

In laptop modem applications, the 89C024LT chip set along with a Data Access Arrangement (DAA), a single 8-bit EPROM, and an 8K x 8 static RAM represent the circuitry required for implementing an auto-dial, auto-answer, 300 to 2400 bps, MNP class 5 full duplex intelligent modem. Refer to Figure 2 for a block diagram of this application.

A complete set of Industry Standard AT commands is provided for modem configuration and user interface. Additional commands have been implemented for power down modes and MNP feature control. Virtually all PC software written for the AT command set can also be used with this chip set. Alternatively, in applications where user proprietary modem control commands and features are desired, the user can replace the 89C024LT command module with custom proprietary software.

The 89C024LT has a set of default features. Upon power up, the modem configuration will be in accordance with these default options, unless a different configuration has been saved in optional external NVRAM with the &W command.

The 89C024LT modem has built in auto-dialing and auto-answering capabilities. It can be configured to the proper line signaling mode (Tone or Pulse), and to the type (CCITT or Bell) and speed of the calling or answering modem. It can also detect and identify call set-up signals of telephone networks, allowing unattended data call operation.

A full set of diagnostic loop-test features compatible with CCITT V.54 is supported. The chip set also provides a line signal for audio monitoring of call progress, a comprehensive set of DAA control lines for a simple interface to the telephone network, and a full complement of TTL level RS-232/V.24 handshake signals.

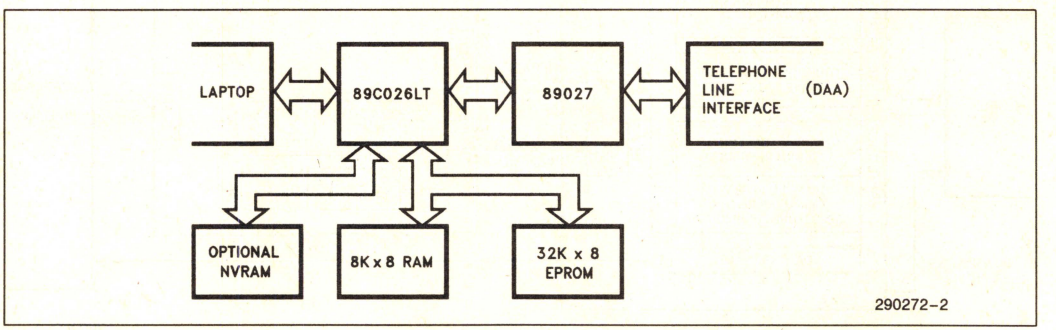

Figure 2. 89C024LT Laptop Modem Application

PACKAGING

89027 is available in PLCC and standard plastic DIP packages. The 89C026LT is available in a PLCC package. Packages are shown from top view, looking down on component side of PC board.

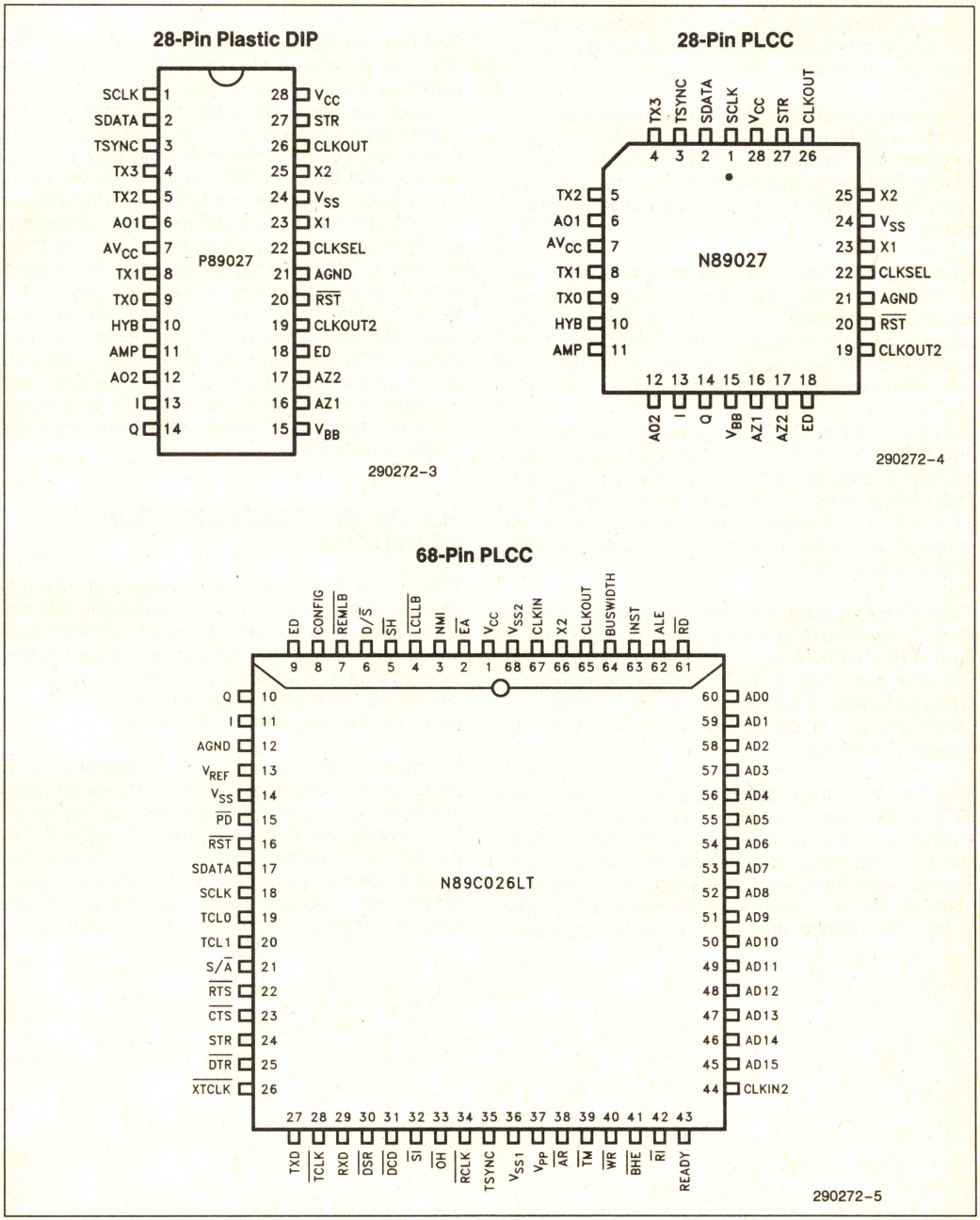

Figure 3. Device Packages

CALL ESTABLISHMENT, TERMINATION AND RETRAIN

The 89C024LT modem system incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The modem chip set has a built-in auto-dialer, both DTMF and Pulse type. It can detect dial, busy, and ringback signals from the remote end, and will provide call progress messages to the user. The modem is also capable of re-dialing the last number dialed.

The modem, when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, and then transmit the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be setup by manual dialing. A transition from voice (i.e., for the purpose of manual dialing) to data mode can be done by the use of a mechanical switch (exclusion key) on the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22 bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests, originated by the remote modem, are of two types, (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip set can also be configured to transmit "long-space" just before disconnection.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22 bis to 212A), the Intel chip set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22 bis standard, transparently, to 212A users. Similarly, a user with a 89C024LT based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C024LT commands and registers that may be used while configuring the modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered separately or in string fashion. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the 'backspace' key (CNTRL H) can be used to correct any error. Upper case or lower case characters can be used in the commands. Commands described in the following paragraphs refer to asynchronous terminals using ASCII codes.

Table 1. Remote Modem Compatibility

Originating 89C024LT Modem		Answering Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89C024LT Modem		Originating Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

* These connection data rates are obtained when connecting 89C024LT based modems end to end. The same results may not be obtained when a 89C024LT based modem is connected to other modems.

Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 300 and 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ; @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code

MNP Feature Control Command Set

\An	Maximum MNP Block Size
%An	Set Auto-Reliable Fallback Character
\Bn	Transmit Break
\Cn	Set Auto-Reliable Buffer
%Cn	Set MNP Compression
\Gn	Set Modem Port Flow Control
\Jn	Bits per Second Rate Adjust
\Kn	Set Break Control
\Nn	Set Operating Mode
\O	Originate Reliable Link
\Qn	Set Serial Port Flow Control
\S	View Active Configuration
\Tn	Set Inactivity Timer
\U	Accept Reliable Link
\Vn	Modify Result Code Form
\Xn	Set XON/XOFF Pass-Through
\Y	Switch to Reliable Mode
\Z	Switch to Normal Mode

& Command Set

&Cn	DCD Options
&Dn	DTR Options
&Fn	Fetch Factory Configuration Profile
&Gn	Guard Tone
&Jn	Telephone Jack Selection
&Ln	Leased/Dial-up Line Selection
&Mn	Async/Sync Mode Selection
&Pn	Make/Break Pulse Ratio
&Rn	RTS/CTS Options
&Sn	DSR Options
&Tn	Test Commands
&Wn	Write Configuration to Non Volatile Memory
&Xn	Sync Clock Source
&Yn	Default NVRAM Profile Select
&Zn	Store Telephone Number

+ Command Set

+En	Disable/Enable Power Down
+Tn	Time to Power Down

CONFIGURATION REGISTERS

The modem stores all the configuration information in a set of registers. Some registers are dedicated to a special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11 *	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register
S31 *	Bit Mapped Options Register

NOTE:
* These S registers can be stored in the NVRAM.

DIALING

Dial modifiers are available for adding conditions to dialed phone numbers.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z0 = T 1 (602) 555-1212
Modem: OK

Result: Modem stores the Tone Dial (T) modifier and phone number T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS0
Modem: T16025551212

Result: Modem dials phone number and attempts to establish a connection.

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

POWER MANAGEMENT

The flexible power management controls allow for a variety of command and hardware driver options. The power down sequence is initiated by placing a logic "low" on pin 15 ($\overline{PD}$) of the 89C026LT. The laptop can control the $\overline{PD}$ signal directly. If such a signal is unavailable, $\overline{PD}$ can be controlled by communications software via $\overline{DTR}$. Lack of data activity or an in-coming ring signal can also be used to control $\overline{PD}$.

Placing the crystal on the 89C026LT (Figure 10) allows it to reduce power consumption by turning off the oscillator. When online and connected to a remote modem, the power consumption for the 89C024LT is typically 400 mW. Additionally, when the 89027 is not needed (on-hook, not connected to a remote modem) the 89C026LT places it in standby. In standby the chip set power consumption is typically 255 mW. When powered down via the $\overline{PD}$ pin on the 89C026LT, the chip set typically consumes 5 mW. Minimum memory-system power-consumption can be achieved by chip selecting memory only when addressed.

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 4. The DAA section shown in this diagram may be implemented using the suggested diagram in Figure 5. Figure 6 shows the use of the power-down feature.

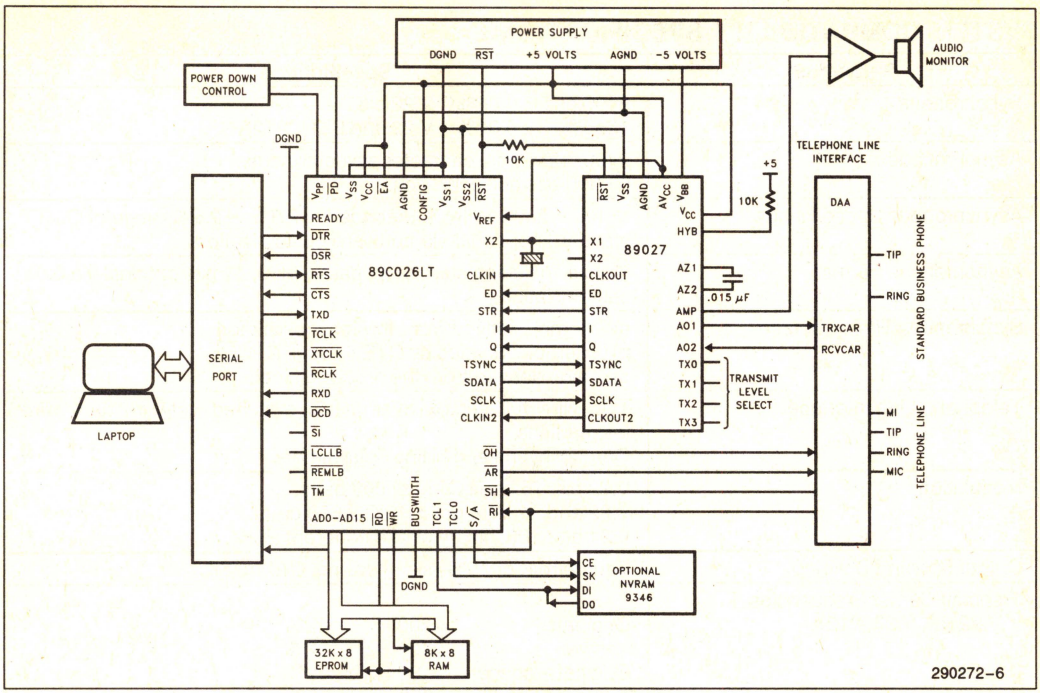

Figure 4. Typical Laptop Modem

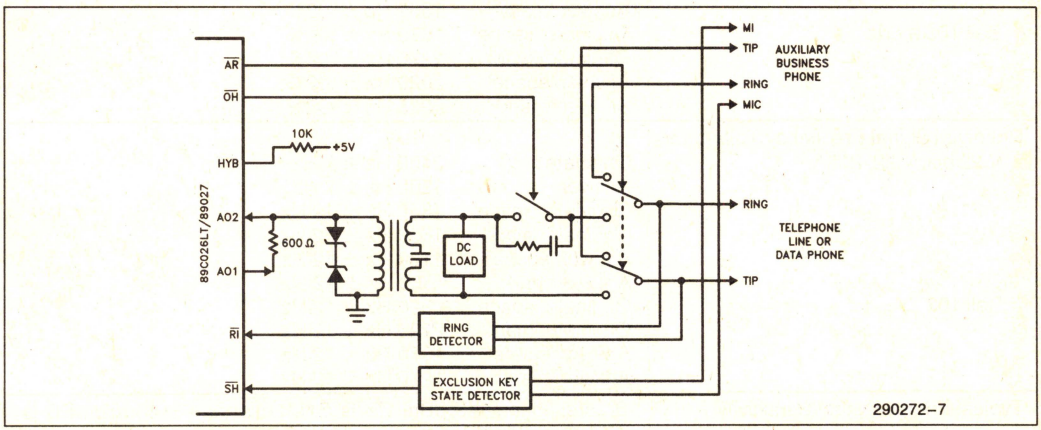

Figure 5. Typical Telephone Line Interface Using Internal Hybrid

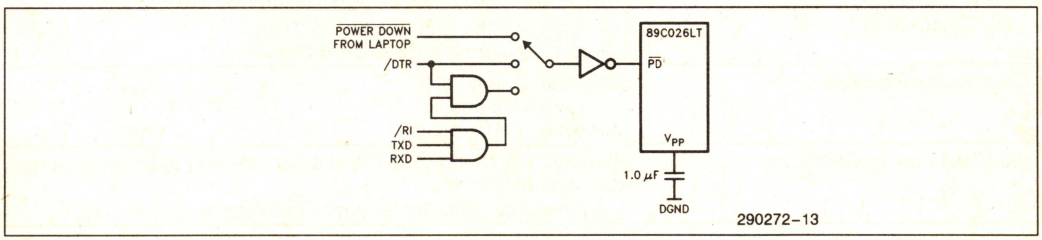

Figure 6. Power-Down Control

SYSTEM COMPATIBILITY SPECIFICATIONS

Parameter	Specification
Synchronous	2400 bps ±0.01% V.22 bis 1200 bps ±0.01% V.22 and BELL 212A
Asynchronous	2400, 1200 bps, character asynchronous. 0 - 300 bps anisochronous.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. (8, 9, 11 bits optional via S/W customization.)
Synchronous Timing Source	a) Internal, derived from the local oscillator. b) External, provided by DTE through $\overline{\text{XTCLK}}$. c) Slave, derived from the received clock.
Telephone Line Interface	Two wire full duplex over public switched network or 4 wire leased lines. On-chip hybrid and billing delay timers.
Modulation	V.22 bis, 16 point QAM at 600 baud. V.22 and 212A, 4 point PSK at 600 baud. V.21 and 103, binary phase coherent FSK
Output Spectral Shaping	Square root of 75% raised cosine, QAM/PSK.
Transmit Carrier Frequencies V.22 bis, V.22, 212A V.21 Bell 103 mode	 Originate 1200 Hz ± .02% Answer 2400 Hz ± .02% Originate 'space' 1180 Hz ± .02% Originate 'mark' 980 Hz ± .02% Answer 'space' 1850 Hz ± .02% Answer 'mark' 1650 Hz ± .02% Originate 'space' 1070 Hz ± .02% Originate 'mark' 1270 Hz ± .02% Answer 'space' 2020 Hz ± .02% Answer 'mark' 2225 Hz ± .02%
Received Signal Frequency Tolerance V.22 bis, V.22, 212A V.21 Bell 103	 Originate 2400 Hz ± 7 Hz Answer 1200 Hz ± 7 Hz Originate 'space' 1850 Hz ± 12 Hz Originate 'mark' 1650 Hz ± 12 Hz Answer 'space' 1180 Hz ± 12 Hz Answer 'mark' 980 Hz ± 12 Hz Originate 'space' 2020 Hz ± 12 Hz Originate 'mark' 2225 Hz ± 12 Hz Answer 'space' 1070 Hz ± 12 Hz Answer 'mark' 1270 Hz ± 12 Hz
Typical Energy Detect Sensitivity	Greater than −43 dBm ED is ON. Less than −48 dBm ED is OFF. Signal in dBm measured at AO2.
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.
Line Equalization	Fixed compromise equalization, transmit. Adaptive equalizer for PSK/QAM, receive.
Diagnostics Available	Local analog loopback. Local digital loopback. Remote digital loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeros' and error detector, to be used along with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	Rx Level (dBm)	Answer (dB)	Originate (dB)
V.22 bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

— Receive Signal (Rx) measured at A02 (transmit level set at −9 dBm)

— Unconditioned 3002 Line

— 3 KHz Flat-Band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10/20		pps	Software Controlled
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	 referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89C026LT OVERVIEW

The 89C026LT processor performs data manipulation, signal processing and user interface functions. It requires a single ROM and RAM to execute standard, and/or custom code with high level protocol functions. A block diagram of the 89C026LT is provided in Figure 7.

89C026LT contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. A UART or USART may be used to transfer data to and from a microcomputer bus. The 89C026LT supports the industry standard AT command set facilitating compatability with most PC software.

During transmit operation, the 89C026LT synthesizes DTMF tones and the 300 BPS FSK modem signal and transmits them to the 89027 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, in the case of asynchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C026LT transmits digitized phase and amplitude samples to 89027 over the high speed serial link.

In the receive operation, the information is received by the 89C026LT from the 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C026LT. By using DSP algorithms, the received signals are processed using adaptive equalization for telephone line delay, amplitude distortion and gain adjustments and the signal demodulated. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

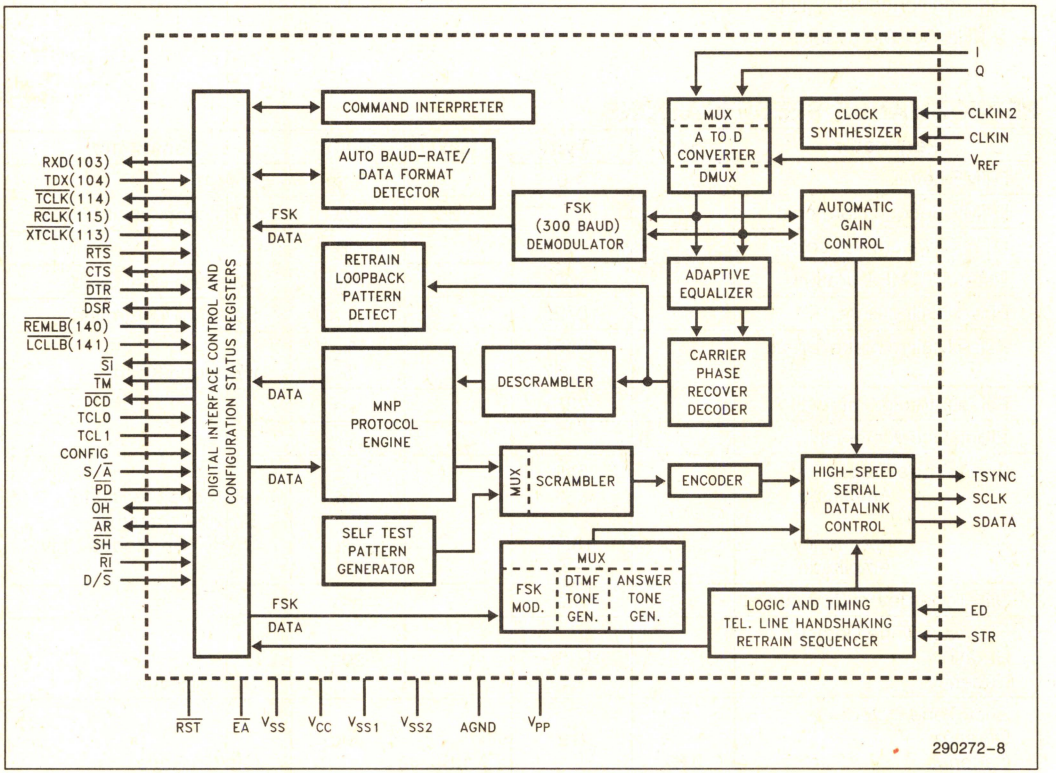

Figure 7. 89C026LT Block Diagram

89C026LT PINOUT

Symbol	Function (89C024LT)	Direction(4)	Pin No.
CLKIN	12.96 MHz master clock from 89027	In	67
CLKIN2	270 KHz from 89027	In	44
$\overline{RST}$	Chip reset (active low)	In	16
I	In-phase received signal	In	11
Q	Quadrature-phase received signal	In	10
STR	Symbol Timing from 89027	In	24
ED	Energy Detect input	In	9
TSYNC	Transmitter sync pulse to 89027	Out	35
SDATA	Serial Data to 89027	Out	17
SCLK	Serial Clock to 89027	Out	18
$\overline{OH}$	Off-Hook control to DAA	Out	33
$\overline{SH}$	Switch-Hook from dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay control to DAA	Out	38
TCL1	NVRAM Data I/O	I/O	20
TCL0	NVRAM CLK	Out	19
$\overline{PD}$	Power-down control	In	15
S/$\overline{A}$	NVRAM $\overline{CE}$	Out	21
D/$\overline{S}$	Dumb/$\overline{Smart}$ mode select	In	6
CONFIG	Reserved for future use (V_{CC})(2)	In	8
$\overline{TM}$	Test Mode Indicator	Out	39
TXD	Transmitted data from DTE	In	27
RXD	Received data to DTE	Out	29
$\overline{RTS}$	Request to send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received clock to DTE	Out	34
$\overline{TCLK}$	Transmit clock to DTE	Out	28
$\overline{XTCLK}$	External timing clock from DTE	In	26
$\overline{SI}$	Speed Indicator to DTE	Out	32
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive power supply (+5V)	+5V	1
V_{SS}	Digital Ground	GND	14
V_{REF}	A/D converter reference	+5V	13
V_{SS1}	Digital ground	GND	36
V_{SS2}	Digital ground	GND	68
AGND	Analog ground	AGND	12
V_{PP}	Timing pin for return from power-down	In	37
$\overline{EA}$	External Memory enable	In	2
AD0-AD15	External memory access address/data(3)	I/O	60–45
$\overline{AA}$	Auto Answer(3)	Out	60
$\overline{JS}$	Jack Select(3)	Out	59
$\overline{CD}$	Carrier Detect Indicator(3)	Out	58
$\overline{MR}$	Modem Ready Indicator(3)	Out	57
$\overline{REL}$	MNP Reliable Link Active(3)	Out	56
$\overline{CLASS5}$	MNP Class 5 Compression Active(3)	Out	55
$\overline{ERR}$	Error detected by MNP(3)	Out	54

89C026LT PINOUT (Continued)

Symbol	Function (89C026LT)	Direction(4)	Pin No.
NMI	Non-maskable Interrupt(V_{SS})(1)	In	3
X2	Crystal output	Out	66
CLKOUT	Clk output	Out	65
BUSWIDTH	Bus Width	In	64
INST	External memory instruction fetch	Out	63
ALE	Address latch enable	Out	62
$\overline{RD}$	External memory read	Out	61
READY	External memory ready	In	43
$\overline{BHE}$	External memory bus high enable	Out	41
$\overline{WR}$	External memory write	Out	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (V_{CC}) must be connected to V_{CC}.
3. AD0–AD3 are used as $\overline{AA}$, $\overline{JS}$, $\overline{CD}$, $\overline{MR}$, $\overline{REL}$, $\overline{CLASS\ 5}$, and $\overline{ERR}$ respectively.
4. Pins with direction "IN" must not be left floating.

89C026LT PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89C026LT samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89C026LT as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. A logic 'high' is mark. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

$\overline{PD}$

Power-down control. A low on this input pin, in conjunction with the +En and +Tn commands, will cause the modem to go into a power-down mode.

V_{PP}

Timing pin for return from power-down. Connect a 1.0 μf capacitor between V_{PP} and V_{SS} if the power-down option is used. This capacitor causes an internal timing circuit to give the oscillator time to stabilize before turning on internal clocks. This pin may be left floating or connected through a 1.0 μF capacitor to V_{SS} if power-down mode is not required.

$\overline{TM}$

A low indicates maintenance condition in the modem.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

A low indicates modem is off-hook, is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a low-to-high transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A low-to-high transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

TCL1, TCL0

These pins are used as the serial clock and data for interface to an NVRAM. Refer to Figure 3. TCL0 is used to output a clock and serial data is transferred in on TCL1.

$\overline{AR}$

This Auxiliary relay control is for switching a relay for voice or data calls. High is voice, low is data.

$\overline{RI}$

A low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high indicates an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins, sets the modem to the local digital loopback.

$\overline{REMLB}$

A low on this pin initiates a remote loopback condition.

$\overline{CD}$

A Low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test mode is active.

$\overline{REL}$

A low indicates that an MNP reliable link has been established.

$\overline{CLASS5}$

A low indicates that MNP Class 5 (data compression) is in operation.

$\overline{ERR}$

Goes low for 1 second whenever MNP detects an error.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 BELL) or range of rates. High selects the Low rate or range of rates.

D/$\overline{S}$

A low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89027 AVcc.

V_{SS}

This pin must be connected to Digital Ground.

S/$\overline{A}$

The function of this pin is re-defined as external NVRAM CE.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory. This pin must be tied high.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

BUSWIDTH

When high, external memory accesses are 16 bits wide. When low, external memory accesses are 8 bits wide. This pin must be tied low.

READY

When high, no wait states are inserted in external memory accesses. When low, one wait state is inserted in each external memory access.

89C026LT ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −40°C to +125°C
Voltage from Any Pin to V_{SS} or AGND ..... −0.5V to +7.0V
Average Output Current from Any Pin ..... 10 mA
Power Dissipation ..... 1.5 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
f_{OSC}	CLKIN Frequency	12.95870	12.96130	MHz

NOTE:
The AGND and V_{SS} on both the 89C026LT and the 89027 must be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on CLKIN	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage(4)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage(3)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA
I_{LI}	Input Leakage Current(5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current(6)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current(3)			−50	μA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current in RESET(2) (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, INST, SCLK)			−7	mA	V_{IN} = 0.45V

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
I_{REF}	A/D Converter Reference Current		2	5	mA	CLKIN = 12.96 MHz $V_{CC} = V_{PP} = V_{REF} = 5.25$
I_{CC1}	Active Mode Current (Typical)		45	60	mA	CLKIN = 12.96 MHz
R_{RST}	RESET Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	f_{TEST} = 1.0 MHz
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.25$

NOTES:
(Notes apply to all specifications)
1. All pins except RESET and CLKIN.
2. Holding these pins below V_{IH} in RESET may cause the part to enter test modes.
3. TCL0, TCL1, S/$\overline{A}$, RTS, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{SI}$, $\overline{OH}$.
4. $\overline{BHE}$, INST, CLKOUT, RESET, $\overline{TCLK}$, RXD, $\overline{RCLK}$, TSYNC, $\overline{TM}$, SCLK, SDATA. The V_{OH} specification is not valid for RESET.
5. EA, READY, BUSWIDTH, NMI, STR, DTR, XTCLK, TXD, B/C, CLKIN2, and RI.
6. S/D, $\overline{SH}$, $\overline{REMLB}$, $\overline{LCLLB}$, I, Q, CONFIG, ED.
7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.

AC CHARACTERISTICS (Over specified operating conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} 12.96 MHz

This system must meet these specifications to work with 89C026LT:

Symbol	Parameter	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 60$	ns	
T_{YLYH}	Non READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 3)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTE:
1. If max is exceeded, additional wait states will occur.
2. $T_{AVDV} = 3T_{OSC} - 67 + 2T_{OSC}$ (for 1 wait state)
3. $T_{RLDV} = T_{OSC} - 23 + 2T_{OSC}$ (for 1 wait state)

AC CHARACTERISTICS (Continued)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} 12.96 MHz

The 89C026LT will meet these specifications:

Symbol	Parameter	Min	Max	Units	Notes
F_{CLKIN}	Oscillator Frequency	12.95870	12.96130	MHz	
T_{OSC}	Oscillator Period	$1/F_{CLKIN(MAX)}$	$1/F_{CLKIN(MIN)}$	ns	
T_{XHCH}	F_{CLKIN} High to CLKOUT High or Low	40	110	ns	(Note 1)
T_{CLCL}	CLKOUT Cycle Time	$2\,T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	15	ns	
T_{LHLH}	ALE Cycle Time	$4\,T_{OSC}$		ns	
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 20$		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 35$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$	$T_{OSC} + 25$	ns	
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		10	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 15$	$T_{OSC} + 5$	ns	
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 15$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 15$	$T_{OSC} + 10$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST, Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 15$		ns	
T_{RHBX}	$\overline{BHE}$, INST, Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 30$		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 25$		ns	

NOTES:
1. Typical specifications, not guaranteed.
2. Assuming back-to-back bus cycles.

WAVEFORMS

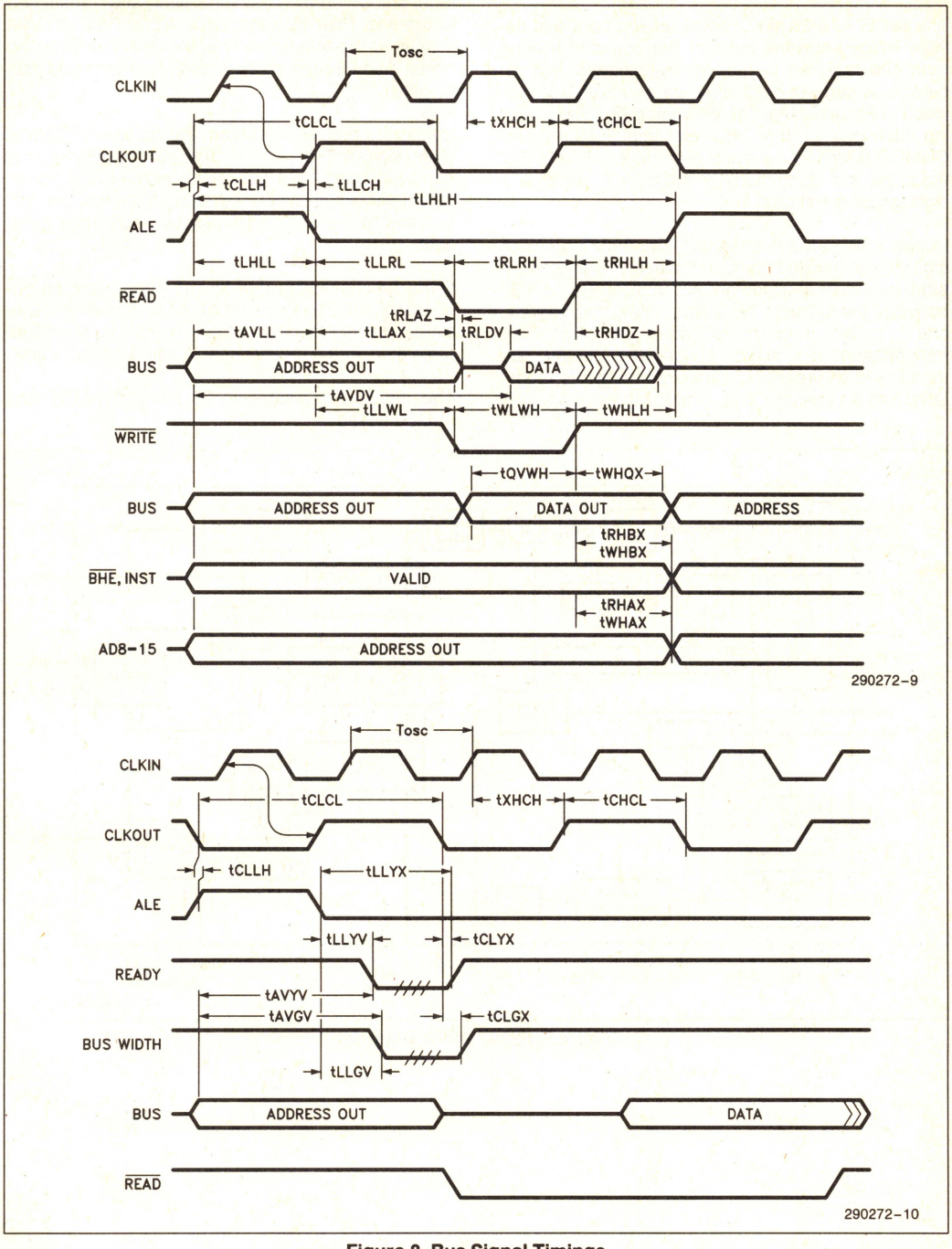

Figure 8. Bus Signal Timings

89027 OVERVIEW

The 89027 is a 28 pin CHMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 9. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89027 functions are controlled by 89C026LT, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89C026LT. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through an on-board programmable gain amplifier.

During the receive operation, the received FSK and QAM signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C026LT processor as analog signals.

Other functions provided by the 89027 are: an on-board two wire to four wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89027 is available in 28 pin plastic DIP and PLCC packages.

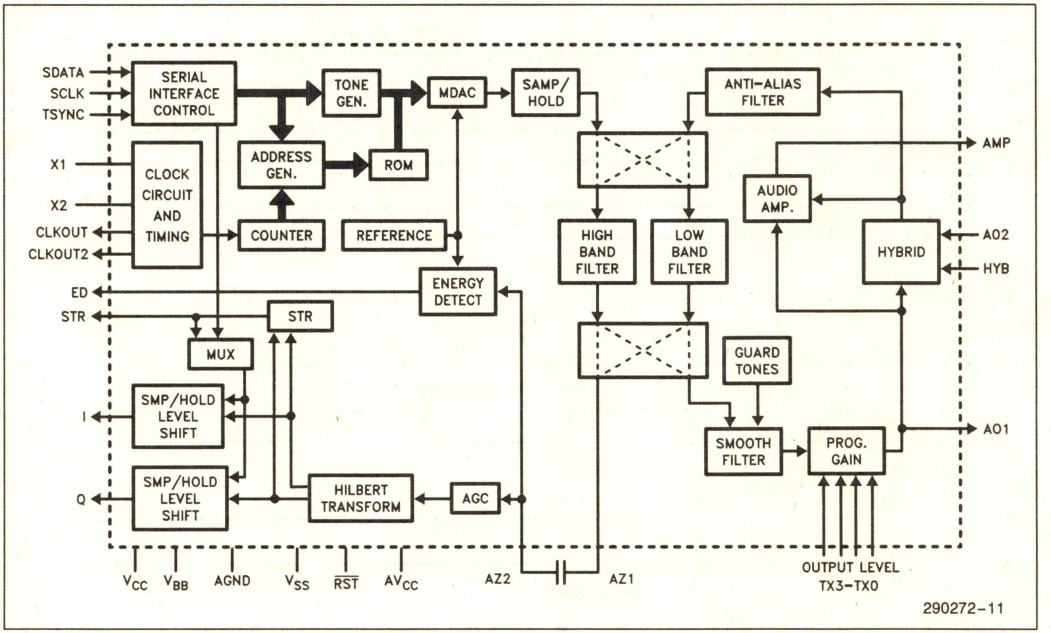

Figure 9. 89027 Block Diagram

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock Output to 89C026LT	Out	26
CLKOUT2	270 KHz Clock Output to 89C026LT	Out	19
$\overline{RST}$	Chip reset (active low)(3)	In	20
HYB	Enable on-chip hybrid(1)	In	10
AZ1	Auto-zero capacitor	Out	16
AZ2	Auto-zero capacitor	In	17
SDATA	Serial data from 89C026LT	In	2
SCLK	Serial clock from 89C026LT	In	1
TSYNC	Transmitter sync from 89C026LT	In	3
STR	Symbol timing to 89C026LT	Out	27
ED	Receiver energy detect to 89C026LT	Out	18
I	In phase received signal to 89C026LT	Out	13
Q	Quadrature-phase received signal to 89C026LT	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control (LSB)(1)	In	9
TX1	Transmitter level control(1)	In	8
TX2	Transmitter level control(1)	In	5
TX3	Transmitter level control (MSB)(1)	In	4
NC	(Note 2)	In	22

NOTE:
1. When held high, these pins must be connected through 10K resistors to V_{CC}.
2. Reserved Pin. Must be left No Connect.
3. Connect to reset circuitry through a 10K resistor.

89027 Pinout Description

TX0-3

These four pins control the transmitted signal level. Refer to Transmit Level Table.

HYB

This pin enables the on-chip hybrid. A line impedance matching network must be connected between AO1 and AO2 when HYB is enabled. If HYB is disabled and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AO1

Transmitter output.

AO2

Receiver input.

AMP

This output can be used to monitor the call progress tones and operation of the line.

ABSOLUTE MAXIMUM RATINGS(2)

Temperature Under Bias ..... 0 to +70° C

Storage Temperature ..... −40 to +125° C

All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V

All Input and Output Voltages with Respect to V_{CC} & AV_{CC} ..... −13.0V to 0.3V

Power Dissipation 1.35W

Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

NOTES:
1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0–TX3 only.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{BB}	Analog Supply Voltage	−4.75	−5.25	V

POWER DISSIPATION Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ± 5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$Alcc_1$	AV_{CC} Operating Current		15	21	mA
Icc_1	V_{CC} Operating Current		5	6	mA
Ibb_1	V_{BB} Operating Current		−15	−21	mA
$Alcc_s$	AV_{CC} Standby Current		0.2	1	mA
Icc_s	V_{CC} Standby Current		5	6	mA
Ibb_s	V_{BB} Standby Current		−0.6	−2	mA
$Alcc_p$	AV_{CC} Power-Down Current		100		μA
Icc_p	V_{CC} Power-Down Current		450		μA
Ibb_p	V_{BB} Power-Down Current		450		μA
Pdo	Operating Power Dissipation		175	250	mW
Pds	Standby Power Dissipation		30	50	mW
Pd_p	Power Down Power Dissipation		5		mW

D.C. CHARACTERISTICS (T_A=0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C026LT power supply. Typical Values are for T_A = 25°C and nominal power supply values. V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C026LT V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: CLKOUT

Symbol	Parameter	Min	Max	Units	Test Conditions
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.4	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50μa, 1 TTL load
Vcol	CLKOUT Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	CLKOUT High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

A.C. CHARACTERISTICS (T_A = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal Level			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V<Vin<+2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20%
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

CRYSTAL REQUIREMENTS(1)

Parameter	Min	Typ	Max	Units	Comments
Frequency Accuracy (0°C–70°C)	−0.0035%	12.96	+0.0035%	MHz	Refer to Figure 10
Rx		10	16	Ohms	
Cx		0.024		pF	
Co	5.1	5.6	6.1	pF	
C_L(2)	−5%	47	+5%	pF	2 Load Capacitors

NOTES:
1. Crystal Type: Parallel Resonant
2. Crystal manufacturers usually specify the accuracy of a parallel resonant circuit at a given "load capacitance". This "load capacitance" is specified to the crystal manufacturer as 33 pf. 33 pf includes the parallel combination of the capacitances seen at the pins of the crystal. These capacitances include C_L, IC pin capacitances, and a 3 ± 2 pf trace capacitance.

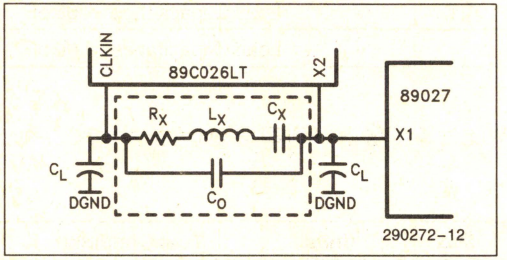

Figure 10. Crystal Equivalent Circuit

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 Ohms kOhms	
Load Capacitance AMP			 100	 pF	
Audio Amp Gain AO1 to Amp		−9 −18 −26 −70		dB dB dB dB	Max Mid Min Off (Software Selectable)
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −60		dB dB dB dB	Max Mid Min Off (Software Selectable)

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

Transmit Output Level(1)		
TX 3,2,1,0	Typ	Units
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK transmit signal levels, they are typically 1 dB lower. All signals are measured at A01. The tolerance for the transmit levels is ±1 dBm.

Reference Manuals

The Modem Reference Manual (Order Number 296235-002) contains pin descriptions, AT and MNP command descriptions, schematics, and important design guidelines for the 89C024LT, 89C024XE, and 89024 modem chip sets. The Modem Software Reference Manual (Order Number 296503-001) provides information about the modem software routines. Contact your local Intel sales office for the latest information.

89C024XE CHIP SET USERS:

Note the following when using the 89C024LT Laptop chip set in place of the 89C024XE:

1. $\overline{PD}$ (B/$\overline{C}$ on 89C024XE) can be left tied to digital V_{CC} or can be connected to the power-down control. If the power down mode is used, a 1.0 μf capacitor must be connected from V_{PP} on the 89C026LT to digital ground.
2. Buswidth pin is tied directly to ground because 89C024LT uses 8-bit EPROM.
3. No 74HC373 latch is required for AD8–AD15 because 89C026LT latches them internally.
4. A single chip select inverter is required from AD15 to select between EPROM and RAM memory.
5. Optional inverter from AD14 can be used to power-down RAM.
6. If minimum power-down currents are not required, the 89C024XE crystal configuration and specifications may be used.

REVISION SUMMARY

The following list represents the differences between version -005 and version -004 of the 80C024LT Error Correcting Laptop Modem Chip Set Data Sheet. These changes reflect the device characteristics changes due to the P645 to P629.1 process conversion.

Packaging

In Figure 3., Device Packages, pin 14, Clock Detect Enable (CDE), has been changed to V_{SS}.

Applications Overview

In Figure 4., Typical Laptop Modem, CDE has been changed to V_{SS}.

89C026LT Overview

In Figure 7., 89C026LT Block Diagram, CDE has been changed to V_{SS}.

89C026LT Pinout

CDE has been changed to V_{SS}.

89C026LT Pin Description

CDE has been changed to V_{SS}, and the paragraph is changed to say that this pin is connected to digital ground.

DC Characteristics

V_{IH1} Min has changed from 2.2V to 2.6V.
I_{IL1} Max has changed from −850 μA to −7 mA.
CDE has been removed from Note 5.

AC Characteristics

T_{AVYV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
T_{LLYV} Max has changed from T_{OSC} − 72 ns to T_{OSC} − 60 ns.
T_{AVGV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
T_{LLGV} Max has changed from T_{OSC} − 70 ns to T_{OSC} − 60 ns.

AC Characteristics (Continued)

T_{AVDV} Max has changed from 5 T_{OSC} − 67 ns to 3 T_{OSC} − 55 ns.
T_{RLDV} Max has changed from 3 T_{OSC} − 23 ns to T_{OSC} − 23 ns.
T_{CLLH} Min has changed from −5 ns to −10 ns, and the Max has changed from 15 ns to 10 ns.
T_{LLRL} Min has changed from T_{OSC} − 40 ns to − 35 ns.
T_{RLCL} Min has changed from 5 ns to 4 ns, and the Max has changed from 30 ns to 25 ns.
T_{CHWH} Min has changed from −10 ns to −5 ns, and the Max has changed from 10 ns to 15 ns.
T_{WLWH} Min has changed from T_{OSC} − 30 ns to T_{OSC} − 15 ns.
T_{WHQX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
T_{WHLH} Min has changed from T_{OSC} − 10 ns to T_{OSC} −15 ns, and the Max has changed from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
T_{WHBX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
T_{WHAX} Min has changed from T_{OSC} − 50 ns to T_{OSC} − 30 ns.

89C024FT
V.42/42bis MODEM CHIP SET

- CHMOS for Low Operating Power
- Low Standby Power
- Minimum Chip Count for Small Size
- V.42 Compliant Error Correction (LAPM and *MNP4)
- V.42bis and MNP5 Data Compression Increase Throughput up to 4 Times with DTE Rates of 9600
- AT Command Set
- V.22bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- Automatically Detects Remote Modem Type and Data Rate
- On-Chip Hybrid
- DTMF and Pulse Dialing
- On-Chip Serial Port and Handshake Signals for RS-232/V.24 Interface
- Serial Interface to External NVRAM
- Automatic Speed Matching in Reliable and Normal Modes
- Hardware and Software Flow Control
- Analog/Digital Loopback Diagnostics
- Synchronous Modes
- Easily Customized Command Set and Features
- Intel's V.42/42bis and MNP Software Co-Developed with R. Scott Associates**
- Packaging:
  - — For Packages
    QN89026FT SV901 68-Pin PLCC
    QP89027 28-Pin PDIP
    Order Kit #89C024FT SZ502
  - — For Packages
    QN89026FT SV901 68-Pin PLCC
    QN89027 28-Pin PLCC
    Order Kit #89C024FT SZ503

(See Packaging Spec. Order #240800-001)

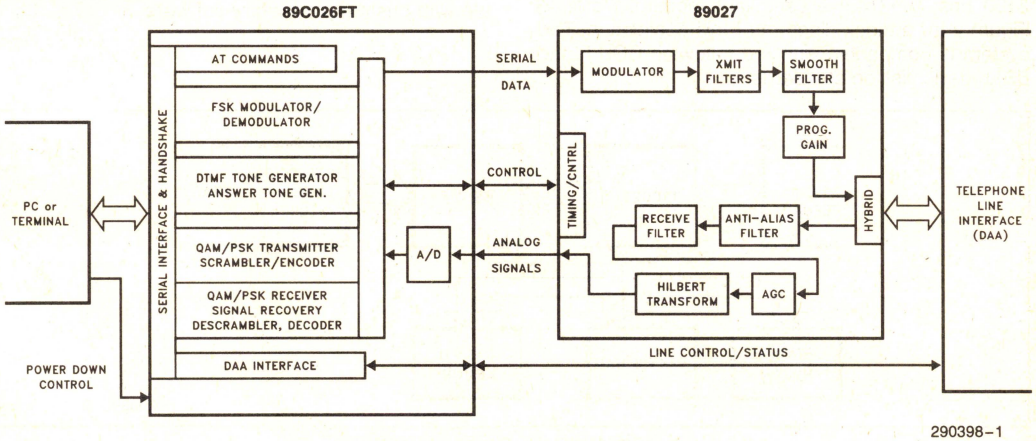

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Figure 1. 89C024FT System Block Diagram

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*MNP is a registered trademark of Microcom, Inc.

**R. Scott Associates, Inc., 5711 Six Forks Road, Suite 301, Raleigh, North Carolina 27609, (919) 846-7171

October 1993
Order Number: 290398-005

GENERAL DESCRIPTION

The Intel 89C024FT is a highly integrated, low power, V.42/42bis compliant modem chip set. This two chip solution is composed of the 89027 analog front end and 89C026FT (an 80C196 based microcontroller).

V.42/42bis compliancy assures adherence to an international error correction (V.42: LAPM and MNP class 4) and data compression (V.42bis: BTLZ and MNP class 5) standards. V.42bis uses BTLZ (British Telecom Lempel Ziv) data compression algorithm to achieve throughputs of up to 4 times the transmission rate, effectively providing up to 9600 bps throughput with a 2400 bps modem.

The benefits of V.42/42bis compliancy are, compatibility with the installed base of MNP class 4 modems, and an increased throughput of up to 4:1. The chip set also provides MNP class 5 operation. This provides 2:1 compression with the large installed base of MNP class 5 modems. These benefits allow the 89C024FT chip set to provide fast and reliable data transfer with the current and upcoming installed base of modems products.

The 89C024FT chip set, along with a Data Access Arrangement (DAA), a single 64K x 8 EPROM, a 32K x 8 static RAM, represent the circuitry necessary for implementing an auto dial/answer, 300 to 2400 bps, V.42/42bis compliant modem. Refer to Figure 2 for a block diagram of this application. The system is compatible with the following CCITT and BELL transmission standards:

- CCITT V.22bis
  2400 bps sync and async
  1200 bps sync and async
- CCITT V.22 A and B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous

This chip set supports power-down modes that are selected via the AT command set, providing flexible power-down management control. The power-down modes make the 89C024FT a good fit for laptop computer applications. Power consumption for the chip set is typically 400 mW during a connection. When powered-down, the chip set consumes 5 mW.

A complete set of industry standard AT commands are provided for modem configuration and user interface. Additional commands have been implemented for power down modes and V.42/42bis/MNP feature control. Virtually all PC software written for the AT command set can also be used with this chip set. Alternatively, in applications where user proprietary modem control commands and features are desired, the user can replace the 89C024FT command module with custom proprietary software.

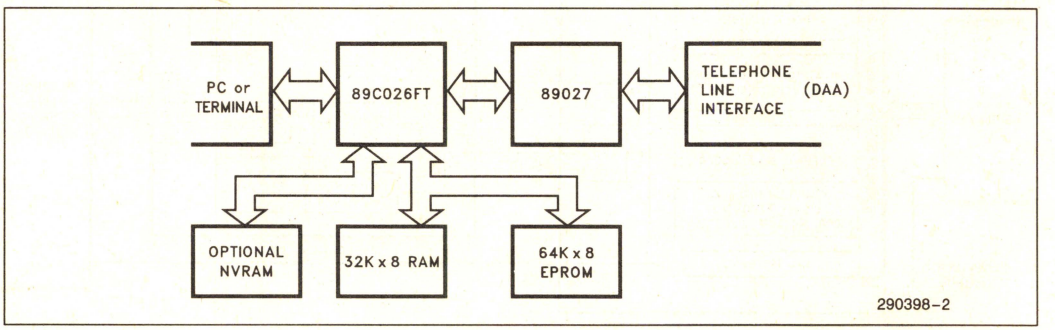

Figure 2. 89C024FT Laptop Modem Application

PACKAGING

89027 is available in PLCC and standard plastic DIP packages. The 89C026FT is available in a PLCC package. Packages are shown from top view, looking down on component side of PC board.

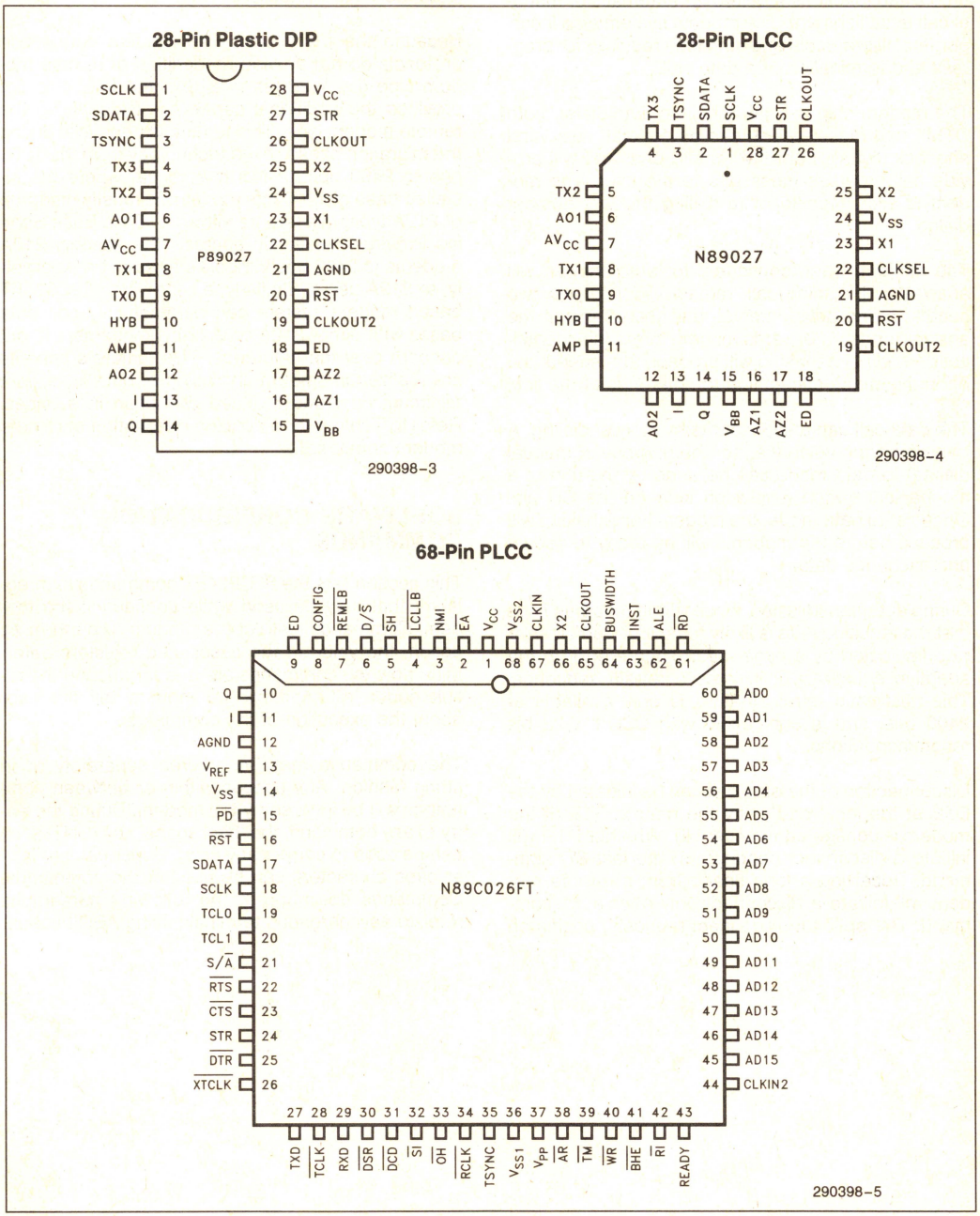

Figure 3. Device Packages

CALL ESTABLISHMENT, TERMINATION AND RETRAIN

The 89C024FT modem system incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The modem chip set has a built-in auto-dialer, both DTMF and Pulse type. It can detect dial, busy, and ringback signals from the remote end, and will provide call progress messages to the user. The modem is also capable of re-dialing the last number dialed.

The modem, when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, and then transmit the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be setup by manual dialing. A transition from voice (i.e., for the purpose of manual dialing) to data mode can be done by the use of a mechanical switch (exclusion key) on the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22 bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests, originated by the remote modem, are of two types, (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip set can also be configured to transmit "long-space" just before disconnection.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22 bis to 212A), the Intel chip set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22 bis standard, transparently, to 212A users. Similarly, a user with a 89C024FT based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C024FT commands and registers that may be used while configuring the modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered separately or in string fashion. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the 'backspace' key (CNTRL H) can be used to correct any error. Upper case or lower case characters can be used in the commands. Commands described in the following paragraphs refer to asynchronous terminals using ASCII codes.

Table 1. Remote Modem Compatibility

Originating 89C024FT Modem		Answering Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89C024FT Modem		Originating Modem Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

* These connection data rates are obtained when connecting 89C024FT based modems end to end. The same results may not be obtained when a 89C024FT based modem is connected to other modems.

1

Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 300 and 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ; @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code
%N	Maximum Line (DCE) Rate
&Cn	DCD Options
&Dn	DTR Options
&Fn	Fetch Factory Configuration Profile
&Gn	Guard Tone
&Jn	Telephone Jack Selection
&Ln	Leased/Dial-up Line Selection
&Mn	Async/Sync Mode Selection
&Pn	Make/Break Pulse Ratio
&Rn	RTS/CTS Options
&Sn	DSR Options
&Tn	Test Commands

Command Set (Continued)

&Wn	Write Configuration to Non Volatile Memory
&Xn	Sync Clock Source
&Yn	Default NVRAM Profile Select
&Zn	Store Telephone Number

V.42/42bis Feature Control Commands

−Jn	V.42 Detection Phase Control
"Hn	V.42bis Compression Control
"Nn	V.42bis Dictionary Size
"On	V.42bis Dictionary Sizing Length

MNP Feature Control Command Set

\An	Maximum MNP Block Size
%An	Set Auto-Reliable Fallback Character
\Bn	Transmit Break
\Cn	Set Auto-Reliable Buffer
%Cn	Set MNP Compression
\Gn	Set Modem Port Flow Control
\Jn	Bits per Second Rate Adjust
\Kn	Set Break Control
\Nn	Set Operating Mode
\O	Originate Reliable Link
\Qn	Set Serial Port Flow Control
\S	View Active Configuration
\Tn	Set Inactivity Timer
\U	Accept Reliable Link
\Vn	Modify Result Code Form
\Xn	Set XON/XOFF Pass-Through
\Y	Switch to Reliable Mode
\Z	Switch to Normal Mode

Power Down Commands

+En	Disable/Enable Power Down
+Tn	Time to Power Down

CONFIGURATION REGISTERS

The modem stores all the configuration information in a set of registers. Some registers are dedicated to a special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11 *	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register
S31 *	Bit Mapped Options Register
S37	Maximum Line (DCE) Rate
S100	Mean Error Monitor Register

NOTE:
* These S registers can be stored in the NVRAM.

DIALING

Dial modifiers are available for adding conditions to dialed phone numbers.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z0 = T 1 (602) 555-1212
Modem: OK

Result: Modem stores the Tone Dial (T) modifier and phone number T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS0
Modem: T16025551212

Result: Modem dials phone number and attempts to establish a connection.

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

POWER MANAGEMENT

The flexible power management controls allow for a variety of command and hardware driver options. The power down sequence is initiated by placing a logic "low" on pin 15 ($\overline{PD}$) of the 89C026FT. The laptop can control the $\overline{PD}$ signal directly. If such a signal is unavailable, $\overline{PD}$ can be controlled by communications software via $\overline{DTR}$. Lack of data activity or an in-coming ring signal can also be used to control $\overline{PD}$.

Placing the crystal on the 89C026FT (Figure 10) allows it to reduce power consumption by turning off the oscillator. When online and connected to a remote modem, the power consumption for the 89C024FT is typically 400 mW. Additionally, when the 89027 is not needed (on-hook, not connected to a remote modem) the 89C026FT places it in standby. In standby the chip set power consumption is typically 255 mW. When powered down via the $\overline{PD}$ pin on the 89C026FT, the chip set typically consumes 5 mW. Minimum memory-system power-consumption can be achieved by chip selecting memory only when addressed.

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 4. The DAA section shown in this diagram may be implemented using the suggested diagram in Figure 5. Figure 6 shows the use of the power-down feature.

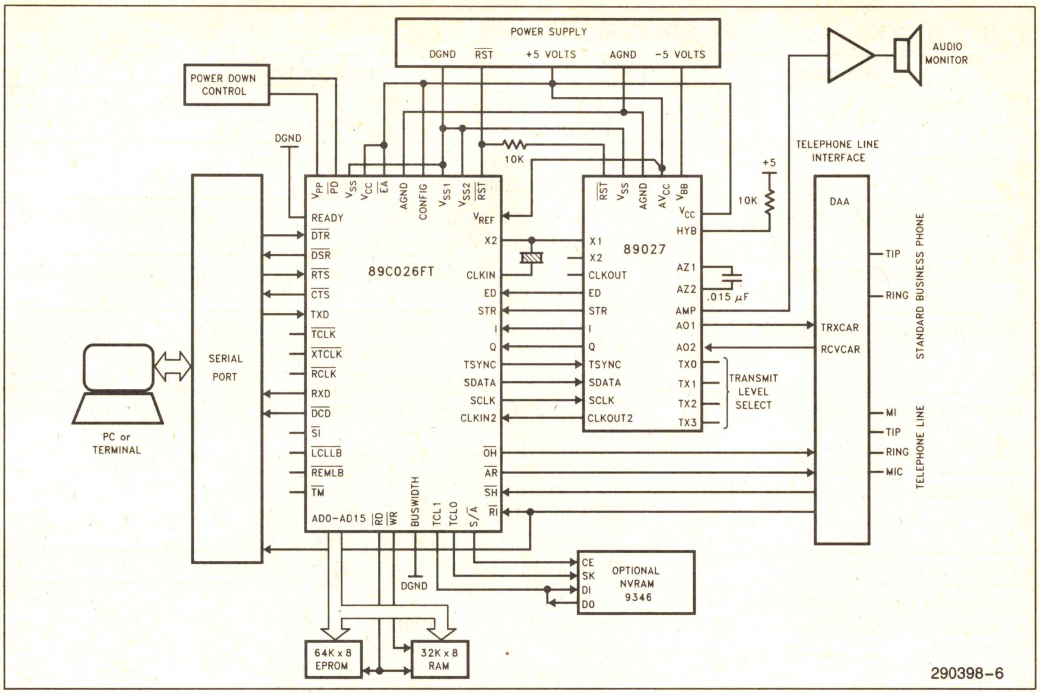

Figure 4. Typical Laptop Modem

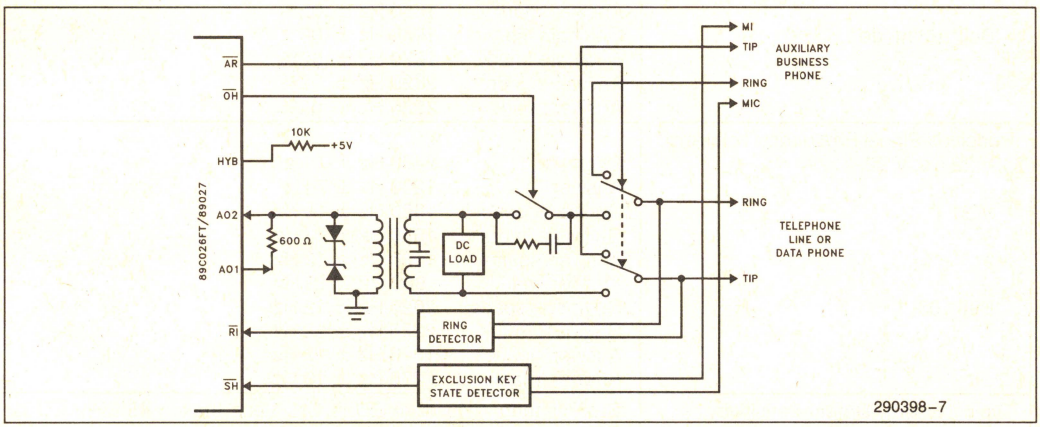

Figure 5. Typical Telephone Line Interface Using Internal Hybrid

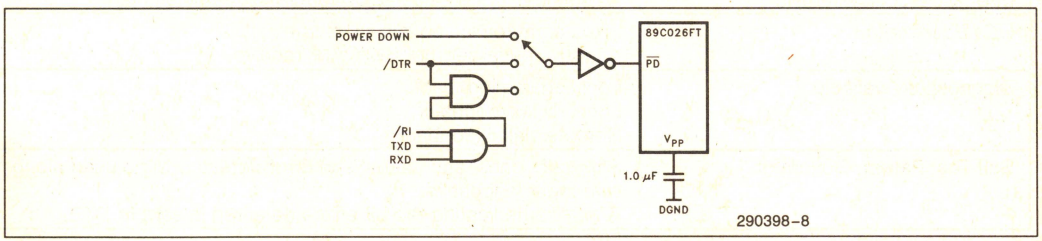

Figure 6. Power-Down Control

SYSTEM COMPATIBILITY SPECIFICATIONS

Parameter	Specification
Synchronous	2400 bps ±0.01% V.22 bis 1200 bps ±0.01% V.22 and BELL 212A
Asynchronous	2400, 1200 bps, character asynchronous. 0 - 300 bps anisochronous.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. (8, 9, 11 bits optional via S/W customization.)
Synchronous Timing Source	a) Internal, derived from the local oscillator. b) External, provided by DTE through $\overline{\text{XTCLK}}$. c) Slave, derived from the received clock.
Telephone Line Interface	Two wire full duplex over public switched network or 4 wire leased lines. On-chip hybrid and billing delay timers.
Modulation	V.22 bis, 16 point QAM at 600 baud. V.22 and 212A, 4 point PSK at 600 baud. V.21 and 103, binary phase coherent FSK
Output Spectral Shaping	Square root of 75% raised cosine, QAM/PSK.
Transmit Carrier Frequencies V.22 bis, V.22, 212A V.21 Bell 103 mode	 Originate 1200 Hz ± .02% Answer 2400 Hz ± .02% Originate 'space' 1180 Hz ± .02% Originate 'mark' 980 Hz ± .02% Answer 'space' 1850 Hz ± .02% Answer 'mark' 1650 Hz ± .02% Originate 'space' 1070 Hz ± .02% Originate 'mark' 1270 Hz ± .02% Answer 'space' 2020 Hz ± .02% Answer 'mark' 2225 Hz ± .02%
Received Signal Frequency Tolerance V.22 bis, V.22, 212A V.21 Bell 103	 Originate 2400 Hz ± 7 Hz Answer 1200 Hz ± 7 Hz Originate 'space' 1850 Hz ± 12 Hz Originate 'mark' 1650 Hz ± 12 Hz Answer 'space' 1180 Hz ± 12 Hz Answer 'mark' 980 Hz ± 12 Hz Originate 'space' 2020 Hz ± 12 Hz Originate 'mark' 2225 Hz ± 12 Hz Answer 'space' 1070 Hz ± 12 Hz Answer 'mark' 1270 Hz ± 12 Hz
Typical Energy Detect Sensitivity	Greater than −43 dBm ED is ON. Less than −48 dBm ED is OFF. Signal in dBm measured at AO2.
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.
Line Equalization	Fixed compromise equalization, transmit. Adaptive equalizer for PSK/QAM, receive.
Diagnostics Available	Local analog loopback. Local digital loopback. Remote digital loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeros' and error detector, to be used along with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	Rx Level (dBm)	Answer (dB)	Originate (dB)
V.22 bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

— Receive Signal (Rx) measured at A02 (transmit level set at −9 dBm)

— Unconditioned 3002 Line

— 3 KHz Flat-Band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10/20		pps	Software Controlled
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	 referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2	 1.5	 sec	 Off/On Ratio

89C026FT OVERVIEW

The 89C026FT processor performs data manipulation, signal processing and user interface functions. It requires a single 64K x 8 ROM and 32K x 8 RAM to execute standard, and/or custom code to perform the V.42/42bis and MNP4/5 protocol functions. The ROM and RAM addresses overlap in external memory and are decoded using the INST and AD15 signals. A block diagram of the 89C026FT is provided in Figure 7.

89C026FT contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. A UART or USART may be used to transfer data to and from a microcomputer bus. The 89C026FT supports the industry standard AT command set facilitating compatability with most PC software.

During transmit operation, the 89C026FT synthesizes DTMF tones and the 300 BPS FSK modem signal and transmits them to the 89027 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, in the case of asynchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C026FT transmits digitized phase and amplitude samples to 89027 over the high speed serial link.

In the receive operation, the information is received by the 89C026FT from the 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C026FT. By using DSP algorithms, the received signals are processed using adaptive equalization for telephone line delay, amplitude distortion and gain adjustments and the signal demodulated. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

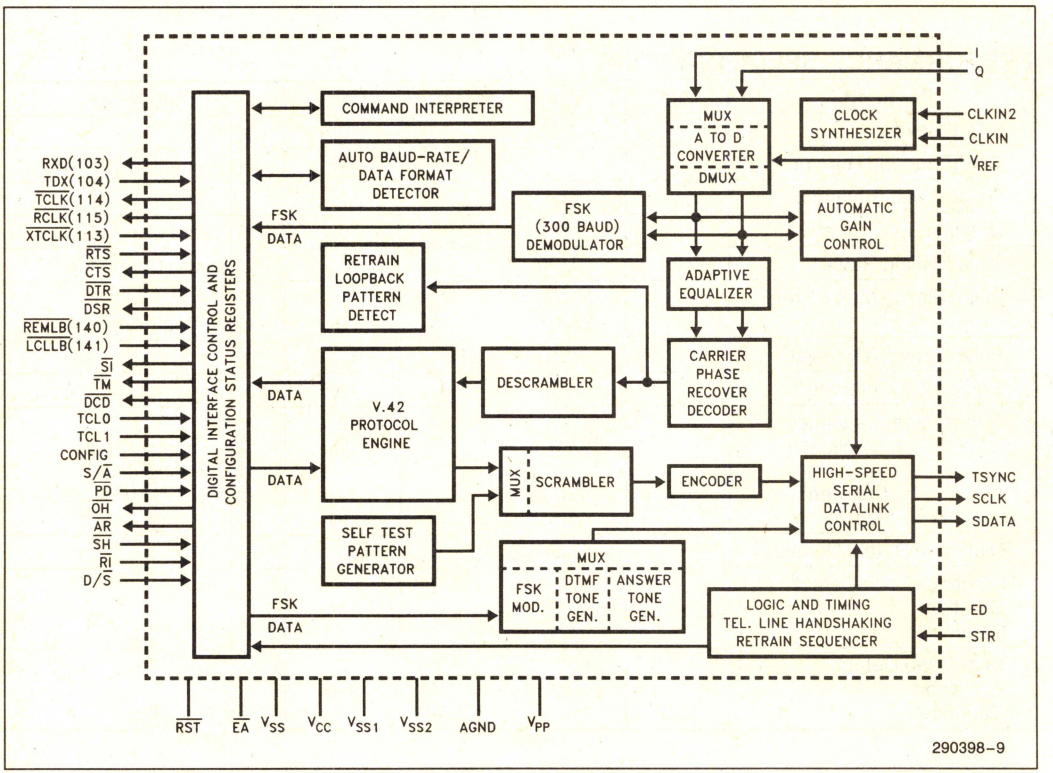

Figure 7. 89C026FT Block Diagram

89C026FT PINOUT

Symbol	Function (89C024FT)	Direction(4)	Pin No.
CLKIN	12.96 MHz master clock from 89027	In	67
CLKIN2	270 KHz from 89027	In	44
$\overline{RST}$	Chip reset (active low)	In	16
I	In-phase received signal	In	11
Q	Quadrature-phase received signal	In	10
STR	Symbol Timing from 89027	In	24
ED	Energy Detect input	In	9
TSYNC	Transmitter sync pulse to 89027	Out	35
SDATA	Serial Data to 89027	Out	17
SCLK	Serial Clock to 89027	Out	18
$\overline{OH}$	Off-Hook control to DAA	Out	33
$\overline{SH}$	Switch-Hook from dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay control to DAA	Out	38
TCL1	NVRAM Data I/O	I/O	20
TCL0	NVRAM CLK	Out	19
$\overline{PD}$	Power-down control	In	15
S/$\overline{A}$	NVRAM $\overline{CE}$	Out	21
D/$\overline{S}$	Dumb/$\overline{Smart}$ mode select	In	6
CONFIG	Reserved for future use (V_{CC})(2)	In	8
$\overline{TM}$	Test Mode Indicator	Out	39
TXD	Transmitted data from DTE	In	27
RXD	Received data to DTE	Out	29
$\overline{RTS}$	Request to send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received clock to DTE	Out	34
$\overline{TCLK}$	Transmit clock to DTE	Out	28
$\overline{XTCLK}$	External timing clock from DTE	In	26
$\overline{SI}$	Speed Indicator to DTE	Out	32
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive power supply (+5V)	+5V	1
V_{SS}	Digital Ground	GND	14
V_{REF}	A/D converter reference	+5V	13
V_{SS1}	Digital ground	GND	36
V_{SS2}	Digital ground	GND	68
AGND	Analog ground	AGND	12
V_{PP}	Timing pin for return from power-down	In	37
$\overline{EA}$	External Memory enable	In	2
AD0-AD15	External memory access address/data(3)	I/O	60–45
$\overline{AA}$	Auto Answer(3)	Out	60
$\overline{JS}$	Jack Select(3)	Out	59
$\overline{CD}$	Carrier Detect Indicator(3)	Out	58
$\overline{MR}$	Modem Ready Indicator(3)	Out	57
$\overline{REL}$	MNP Reliable Link Active(3)	Out	56
$\overline{COMP}$	Compression Active V.42bis or MNP Class 5(3)	Out	55
$\overline{ERR}$	Error detected by LAPM or MNP(3)	Out	54
$\overline{LAPM}$	LAPM Reliable Link Active(3)	Out	53

89C026FT PINOUT (Continued)

Symbol	Function (89C026FT)	Direction(4)	Pin No.
NMI	Non-maskable Interrupt(V_{SS})(1)	In	3
X2	Crystal output	Out	66
CLKOUT	Clk output	Out	65
BUSWIDTH	Bus Width	In	64
INST	External memory instruction fetch	Out	63
ALE	Address latch enable	Out	62
$\overline{RD}$	External memory read	Out	61
READY	External memory ready	In	43
$\overline{BHE}$	External memory bus high enable	Out	41
$\overline{WR}$	External memory write	Out	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (V_{CC}) must be connected to V_{CC}.
3. AD0–AD3 are used as $\overline{AA}$, $\overline{JS}$, $\overline{CD}$, $\overline{MR}$, $\overline{REL}$, $\overline{COMP}$, $\overline{ERR}$, and $\overline{LAPM}$ respectively.
4. Pins with direction "IN" must not be left floating.

89C026FT PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89C026FT samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89C026FT as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. A logic 'high' is mark. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

$\overline{PD}$

Power-down control. A low on this input pin, in conjunction with the +En and +Tn commands, will cause the modem to go into a power-down mode.

V_{PP}

Timing pin for return from power-down. Connect a 1.0 μf capacitor between V_{PP} and V_{SS} if the power-down option is used. This capacitor causes an internal timing circuit to give the oscillator time to stabilize before turning on internal clocks. This pin may be left floating or connected through a 1.0 μF capacitor to V_{SS} if power-down mode is not required.

$\overline{TM}$

A low indicates maintenance condition in the modem.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

A low indicates modem is off-hook, is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a low-to-high transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A low-to-high transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

TCL1, TCL0

These pins are used as the serial clock and data for interface to an NVRAM. Refer to Figure 3. TCL0 is used to output a clock and serial data is transferred in on TCL1.

$\overline{AR}$

This Auxiliary relay control is for switching a relay for voice or data calls. High is voice, low is data.

$\overline{RI}$

A low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high indicates an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins, sets the modem to the local digital loopback.

$\overline{REMLB}$

A low on this pin initiates a remote loopback condition.

$\overline{CD}$

A Low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test mode is active.

$\overline{REL}$

A low indicates that an MNP reliable link has been established.

$\overline{COMP}$

A low indicates that data compression is in operation (V.42bis or MNP Class 5).

$\overline{LAPM}$

A low indicates that a LAPM reliable link has been established.

$\overline{ERR}$

Goes low for 1 second whenever a reliable connection detects an error.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 BELL) or range of rates. High selects the Low rate or range of rates.

D/$\overline{S}$

A low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89027 AVcc.

V_{SS}

This pin must be connected to Digital Ground.

S/$\overline{A}$

The function of this pin is re-defined as external NVRAM CE.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory. This pin must be tied high.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

BUSWIDTH

When high, external memory accesses are 16 bits wide. When low, external memory accesses are 8 bits wide. This pin must be tied low.

READY

When high, no wait states are inserted in external memory accesses. When low, one wait state is inserted in each external memory access.

INST

Output high during an external memory read indicates the read is an instruction fetch. INST is activated only during external memory accesses and output low for data fetch. INST along with AD15 are used to decode the overlapping external ROM and RAM.

89C026FT ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −40°C to +125°C
Voltage from Any Pin to
V_{SS} or AGND ..... −0.5V to +7.0V
Average Output Current from Any Pin ..... 10 mA
Power Dissipation ..... 1.5 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
f_{OSC}	CLKIN Frequency	12.95870	12.96130	MHz

NOTE:
The AGND and V_{SS} on both the 89C026FT and the 89027 must be nominally at the same potential.

D.C. CHARACTERISTICS

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on CLKIN	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage(4)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage(3)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA
I_{LI}	Input Leakage Current(5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current(6)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current(3)			−50	μA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current in RESET(2) (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, INST, SCLK)			−7	mA	V_{IN} = 0.45V

D.C. CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
I_{REF}	A/D Converter Reference Current		2	5	mA	CLKIN = 12.96 MHz $V_{CC} = V_{PP} = V_{REF} = 5.25$
I_{CC1}	Active Mode Current (Typical)		45	60	mA	CLKIN = 12.96 MHz
R_{RST}	RESET Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	f_{TEST} = 1.0 MHz
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.25$

NOTES:
(Notes apply to all specifications)
1. All pins except RESET and CLKIN.
2. Holding these pins below V_{IH} in RESET may cause the part to enter test modes.
3. TCL0, TCL1, S/$\overline{A}$, RTS, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{SI}$, $\overline{OH}$.
4. $\overline{BHE}$, INST, CLKOUT, RESET, $\overline{TCLK}$, RXD, $\overline{RCLK}$, TSYNC, $\overline{TM}$, SCLK, SDATA. The V_{OH} specification is not valid for RESET.
5. EA, READY, BUSWIDTH, NMI, STR, DTR, XTCLK, TXD, B/C, CLKIN2, and RI.
6. S/D, $\overline{SH}$, $\overline{REMLB}$, $\overline{LCLLB}$, I, Q, CONFIG, ED.
7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.

A.C. CHARACTERISTICS (Over specified operating conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} 12.96 MHz

This system must meet these specifications to work with 89C026FT:

Symbol	Parameter	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 60$	ns	
T_{YLYH}	Non READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 3)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTE:
1. If max is exceeded, additional wait states will occur.
2. $T_{AVDV} = 3T_{OSC} - 55 + 2T_{OSC}$ (for 1 wait state).
3. $T_{RLDV} = T_{OSC} - 23 + 2T_{OSC}$ (for 1 wait state).

A.C. CHARACTERISTICS (Continued)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall tines = 10 ns, f_{OSC} 12.96 MHz

The 89C026FT will meet these specifications:

Symbol	Parameter	Min	Max	Units	Notes
F_{CLKIN}	Oscillator Frequency	12.95870	12.96130	MHz	
T_{OSC}	Oscillator Period	$1/F_{CLKIN(MAX)}$	$1/F_{CLKIN(MIN)}$	ns	
T_{XHCH}	F_{CLKIN} High to CLKOUT High or Low	40	110	ns	(Note 1)
T_{CLCL}	CLKOUT Cycle Time	$2\,T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	15	ns	
T_{LHLH}	ALE Cycle Time	$4\,T_{OSC}$		ns	
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 20$		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 35$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$	$T_{OSC} + 25$	ns	
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		10	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 15$	$T_{OSC} + 5$	ns	
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 15$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 15$	$T_{OSC} + 10$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST, Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 15$		ns	
T_{RHBX}	$\overline{BHE}$, INST, Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 30$		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 25$		ns	

NOTES:
1. Typical specifications, not guaranteed.
2. Assuming back-to-back bus cycles.

WAVEFORMS

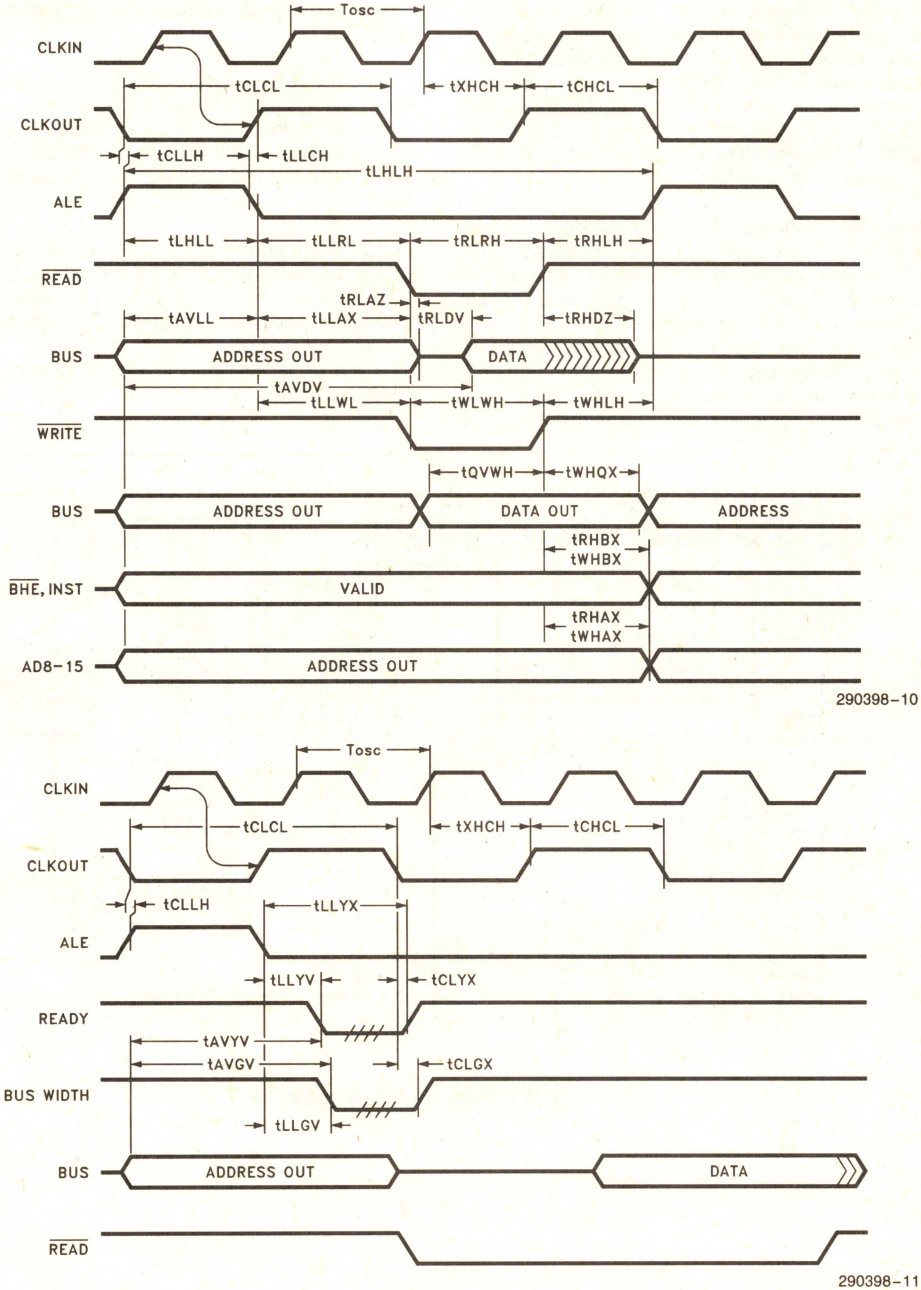

Figure 8. Bus Signal Timings

89027 OVERVIEW

The 89027 is a 28 pin CHMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 9. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89027 functions are controlled by 89C026FT, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89C026FT. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through an on-board programmable gain amplifier.

During the receive operation, the received FSK and QAM signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C026FT processor as analog signals.

Other functions provided by the 89027 are: an on-board two wire to four wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89027 is available in 28 pin plastic DIP and PLCC packages.

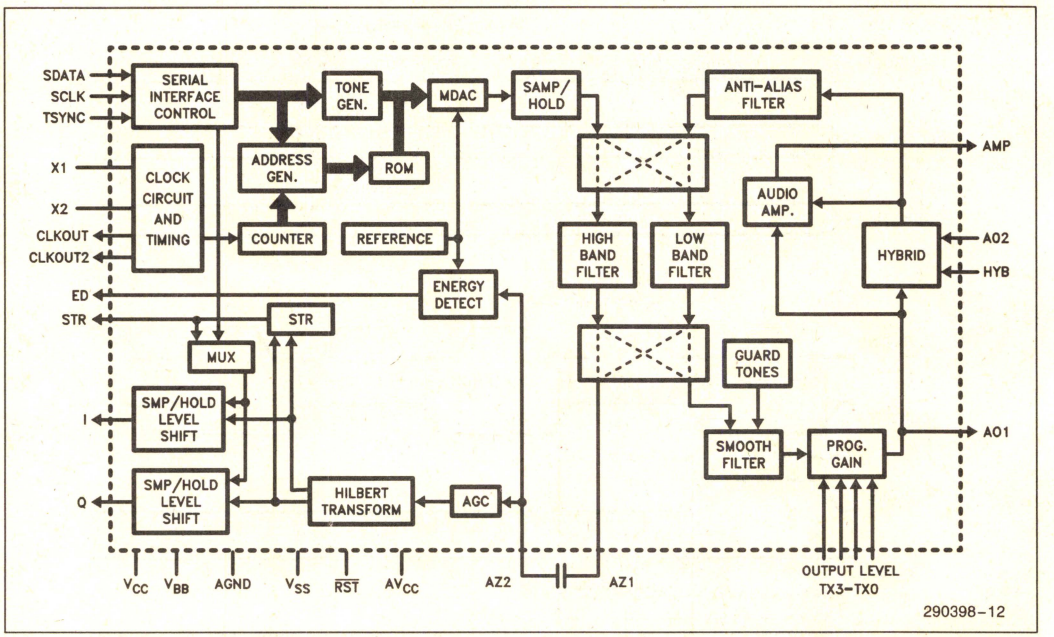

Figure 9. 89027 Block Diagram

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock Output to 89C026FT	Out	26
CLKOUT2	270 KHz Clock Output to 89C026FT	Out	19
$\overline{RST}$	Chip reset (active low)(3)	In	20
HYB	Enable on-chip hybrid(1)	In	10
AZ1	Auto-zero capacitor	Out	16
AZ2	Auto-zero capacitor	In	17
SDATA	Serial data from 89C026FT	In	2
SCLK	Serial clock from 89C026FT	In	1
TSYNC	Transmitter sync from 89C026FT	In	3
STR	Symbol timing to 89C026FT	Out	27
ED	Receiver energy detect to 89C026FT	Out	18
I	In phase received signal to 89C026FT	Out	13
Q	Quadrature-phase received signal to 89C026FT	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control (LSB)(1)	In	9
TX1	Transmitter level control(1)	In	8
TX2	Transmitter level control(1)	In	5
TX3	Transmitter level control (MSB)(1)	In	4
NC	(Note 2)	In	22

NOTE:
1. When held high, these pins must be connected through 10K resistors to V_{CC}.
2. Reserved Pin. Must be left No Connect.
3. Connect to reset circuitry through a 10K resistor.

89027 Pinout Description

TX0-3

These four pins control the transmitted signal level. Refer to Transmit Level Table.

HYB

This pin enables the on-chip hybrid. A line impedance matching network must be connected between AO1 and AO2 when HYB is enabled. If HYB is disabled and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AO1

Transmitter output.

AO2

Receiver input.

AMP

This output can be used to monitor the call progress tones and operation of the line.

ABSOLUTE MAXIMUM RATINGS(2)

Temperature Under Bias ..... 0 to +70° C

Storage Temperature ..... −40 to +125° C

All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V

All Input and Output Voltages with Respect to V_{CC} & AV_{CC} ..... −13.0V to 0.3V

Power Dissipation 1.35W

Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

NOTES:

1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0–TX3 only.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{BB}	Analog Supply Voltage	−4.75	−5.25	V

POWER DISSIPATION Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ± 5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$Alcc_1$	AV_{CC} Operating Current		15	21	mA
Icc_1	V_{CC} Operating Current		5	6	mA
Ibb_1	V_{BB} Operating Current		−15	−21	mA
$Alcc_s$	AV_{CC} Standby Current		0.2	1	mA
Icc_s	V_{CC} Standby Current		5	6	mA
Ibb_s	V_{BB} Standby Current		−0.6	−2	mA
$Alcc_p$	AV_{CC} Power-Down Current		100		μA
Icc_p	V_{CC} Power-Down Current		450		μA
Ibb_p	V_{BB} Power-Down Current		450		μA
Pdo	Operating Power Dissipation		175	250	mW
Pds	Standby Power Dissipation		30	50	mW
Pd_p	Power Down Power Dissipation		5		mW

D.C. CHARACTERISTICS (T_A=0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C026FT power supply. Typical Values are for T_A = 25°C and nominal power supply values. V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C026FT V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: CLKOUT

Symbol	Parameter	Min	Max	Units	Test Conditions
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.4	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50μa, 1 TTL load
Vcol	CLKOUT Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	CLKOUT High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

A.C. CHARACTERISTICS (T_A = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal Level			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V<Vin<+2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20%
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

CRYSTAL REQUIREMENTS(1)

Parameter	Min	Typ	Max	Units	Comments
Frequency Accuracy (0°C–70°C)	−0.0035%	12.96	+0.0035%	MHz	Refer to Figure 10
Rx		10	16	Ohms	
Cx		0.024		pF	
Co	5.1	5.6	6.1	pF	
C_L(2)	−5%	47	+5%	pF	2 Load Capacitors

NOTES:
1. Crystal Type: Parallel Resonant
2. Crystal manufacturers usually specify the accuracy of a parallel resonant circuit at a given "load capacitance". This "load capacitance" is specified to the crystal manufacturer as 33 pf. 33 pf includes the parallel combination of the capacitances seen at the pins of the crystal. These capacitances include C_L, IC pin capacitances, and a 3 ± 2 pf trace capacitance.

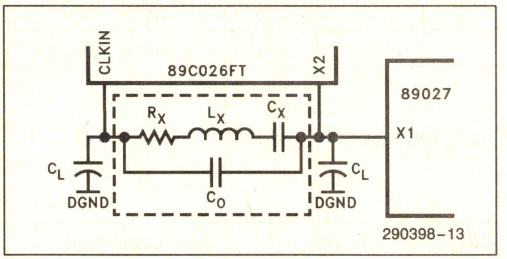

Figure 10. Crystal Equivalent Circuit

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 Ohms kOhms	
Load Capacitance AMP			100	pF	
Audio Amp Gain AO1 to Amp		−9 −18 −26 −70		dB dB dB dB	Max Mid Min Off (Software Selectable)
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −60		dB dB dB dB	Max Mid Min Off (Software Selectable)

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

Transmit Output Level(1)		
TX 3,2,1,0	**Typ**	**Units**
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK transmit signal levels, they are typically 1 dB lower. All signals are measured at A01. The tolerance for the transmit levels is ±1 dBm.

89C024LT CHIP-SET USERS:

An example of how to design a single board for both an 89C024LT and 89C024FT modem product is available from your local Intel sales office. This document is titled "Upgrading from the 89C024LT to 89C024FT". It provides information for a smooth upgrade from an 89C024LT to an 89C024FT product.

REFERENCE MANUALS

The Modem Reference Manual (Order Number 296235-002) contains pin descriptions, AT and MNP command descriptions, schematics, and important design guidelines for the 89C024FT, 89C024XE, and 89024 modem chip sets. The Modem Software Reference Manual (Order Number 296503-001) provides information about the modem software routines. The 89C024FT Modem Reference Manual Addendum contains design information on the 89C024FT chip set. Contact your local Intel sales office for the latest information.

REVISION SUMMARY

The following list represents the differences between version 005 and version 004 of the 80C024FT V.42/42bis Modem Chip Set Data Sheet. These changes reflect the device characteristics changes due the P645 to P629.1 process conversion.

PACKAGING

In Figure 3, Device Packages, pin 14, Clock Detect Enable (CDE), has been changed to V_{SS}.

APPLICATIONS OVERVIEW

In Figure 4, Typical Laptop Modem, CDE has been changed to V_{SS}.

89C026FT OVERVIEW

In Figure 7, 89C026FT Block Diagram, CDE has been changed to V_{SS}.

89C026FT PINOUT

CDE has been changed to V_{SS}.

89C026FT PIN DESCRIPTION

CDE has been changed to V_{SS}, and the paragraph is changed to say that this pin is connected to digital ground.

D.C. CHARACTERISTICS

V_{IH1} Min has changed from 2.2 to 2.6V.

I_{IL1} Max has changed from $-850\ \mu A$ to -7 mA.

CDE has been removed from Note 5.

A.C. CHARACTERISTICS

T_{AVYV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.

T_{LLYV} Max has changed from T_{OSC} − 72 ns to T_{OSC} − 60 ns.

T_{AVGV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.

T_{LLGV} Max has changed from T_{OSC} − 70 ns to T_{OSC} − 60 ns.

T_{AVDV} Max has changed from 5 T_{OSC} − 67 ns to 3 T_{OSC} − 55 ns.

T_{RLDV} Max has changed from 3 T_{OSC} − 23 ns to T_{OSC} − 23 ns.

T_{CLLH} Min has changed from −5 ns to −10 ns, and the Max has changed from 15 ns to 10 ns.

T_{LLRL} Min has changed from T_{OSC} − 40 ns to T_{OSC} − 35 ns.

T_{RLCL} Min has changed from 5 ns to 4 ns, and the Max has changed from 30 ns to 25 ns.

T_{CHWH} Min has changed from −10 ns to −5 ns, and the Max has changed from 10 ns to 15 ns.

T_{WLWH} Min has changed from T_{OSC} − 30 ns to T_{OSC} − 15 ns.

T_{WHQX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.

T_{WHLH} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns, and the Max has changed from T_{OSC} + 15 ns to T_{OSC} + 10 ns.

T_{WHBX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.

T_{WHAX} Min has changed from T_{OSC} − 50 ns to T_{OSC} − 30 ns.

89C124FX
DATA/FAX MODEM CHIP SET

- 9600 bps Send and Receive FAX
- V.29 and V.27ter Compatible
- Supports Communicating Applications Specification (CAS)
- EIA/TIA-578 Compliant FAX Command Set (Service Class 1)
- Compatible with CCITT Group 3 FAX Machines
- 2400 bps Data Modem
- V.22bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- V.42 Compliant Error Correction (LAPM and *MNP4)
- V.42bis and MNP5 Data Compression
- Easy Upgrade from Intel Modem Chip Sets
- AT Command Set
- Minimum Chip Count for Small Size
- CHMOS for Low Operating Power
- Low Standby Power
- On-Chip Hybrid
- DTMF and Pulse Dialing
- Automatic Speed Matching in Reliable and Normal Modes
- Serial Interface to External NVRAM
- Hardware and Software Flow Control
- Analog/Digital Loopback Diagnostics
- Automatically Detects Remote Modem Type and Data Rate
- Easily Customized Command Set and Features
- Synchronous Modes
- On-Chip Serial Port Handshake Signals for RS-232/V.24 Interface
- Packaging
  - — 89127:
    28-Lead PDIP and PLCC, 64-Lead QFP Packages
    Package Type P, N and S
  - — 89C126FX:
    68-Lead PLCC and 80-Lead QFP
    Package Type N and SB

(See Packaging Spec Order No. 240800)

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**R. Scott Associates, Inc., 7701 Six Forks Rd, Suite 120, Raleigh, North Carolina 27615, (919) 846-7171

October 1992
Order Number: 290415-002

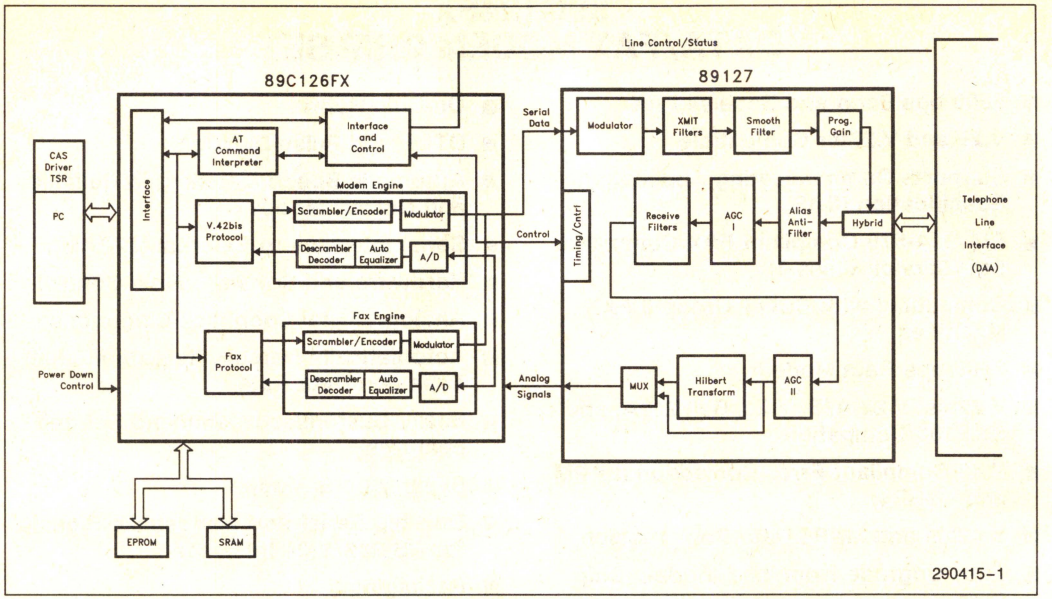


Figure 1. 89C124FX System Block Diagram

GENERAL DESCRIPTION

The Intel 89C124FX is a highly integrated, Send and Receive data-FAX modem chipset. This two chip solution is composed of the 89C126FX microcontroller and the 89127 Analog Front End. The 89C124FX features 9600 bps Send and Receive FAX, V.42/V.42bis error correction and data compression, low power consumption, easy upgrade from other Intel modem chipsets, and ease of use, via the Intel/DCA Communicating Applications Specification (CAS).

The 89C126FX microcontroller executes DSP algorithms for modulation, demodulation, and data formatting. It also performs the AT and EIA/TIA-578 command set interface functions, and error correction and data compression. The 89C126FX comes in a 68-pin PLCC package.

The 89127 AFE provides D/A conversion, filtering, AGC, 2 wire hybrid conversion and telephone line data access arrangement (DAA) interface. The 89127 comes in 28-pin PLCC and 28-pin PDIP packages.

EIA/TIA-578

EIA/TIA-578 is a specification of AT level commands for control of FAX functions. EIA/TIA-578 compliancy assures compatibility with products conforming to this industry standard. EIA/TIA-578 is also known as "Facsimile Service Class 1".

Communicating Applications Specification (CAS)

CAS is a high-level Applications Programmer Interface (API) which: 1) Allows the end user to FAX directly from an application program without using a standalone communications package, and 2) Gives PC-based application software vendors an easy way to include FAX functionality in their products. The 89C124FX supports CAS via a Terminate and Stay Resident (TSR) driver program that resides on the PC. The CAS TSR driver communicates with the 89C124FX via the EIA/TIA-578 interface.

V.42/V.42bis

V.42/42bis compliancy assures adherence to international error correction (V.42: LAPM) and data compression (V.42bis: BTLZ and MNP class 5) standards. V.42bis uses BTLZ (British Telecom Lempel Ziv) data compression algorithm to achieve throughputs of up to 4 times the transmission rate, effectively providing up to 9600 bps throughput with a 2400 bps modem.

V.42/42bis compliancy assures compatibility with the installed base of MNP class 4 modems, and provides an increased throughput of up to 4:1. The chip set also provides MNP class 5 operation. This provides 2:1 compression with the large installed base of MNP class 5 modems. These benefits allow the 89C124FX chip set to provide fast and reliable data transfer with the current and upcoming installed base of modems products.

System Configuration

The 89C124FX chip set, along with a Data Access Arrangement (DAA), a single 128K x 8 EPROM, and a 32K x 8 static RAM, represent the circuitry necessary for implementing a 9600 bps Send/Receive FAX, 2400 bps Data modem with V.42/V.42bis. Refer to Figure 2 for a block diagram of this application. The system is compatible with the following CCITT and Bell transmission standards:

FAX:

- CCITT V.29
  9600 bps async
  7200 bps async
- CCITT V.27ter
  4800 bps async
  2400 bps async

DATA:

- CCITT V.22bis
  2400 bps sync and async
  1200 bps sync and async
- CCITT V.22 A and B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous
- CCITT V.23

Power Down

The 89C124FX chip set supports power-down modes that are selected via the AT command set, providing flexible power-down management control. The power-down modes make the 89C124FX a good fit for laptop and notebook computer applications. Power consumption for the chip set is typically 530 mW during a connection. When powered-down, the chip set consumes 7 mW.

Commands

FAX modem functions are controlled via the EIA/TIA-578 command set. A complete set of industry standard AT commands are provided for configuration and user interface of the data modem functions. Additional commands have been implemented for power down modes, and V.42/42bis/MNP feature control. In applications where user proprietary control commands and features are desired, the user can replace the 89C124FX command module with custom proprietary software.

Optional Features

The 89C124FX supports the addition of a serial EEPROM to store configuration information, LEDs for status indication, and a speaker driver for monitoring the progress of the phone call.

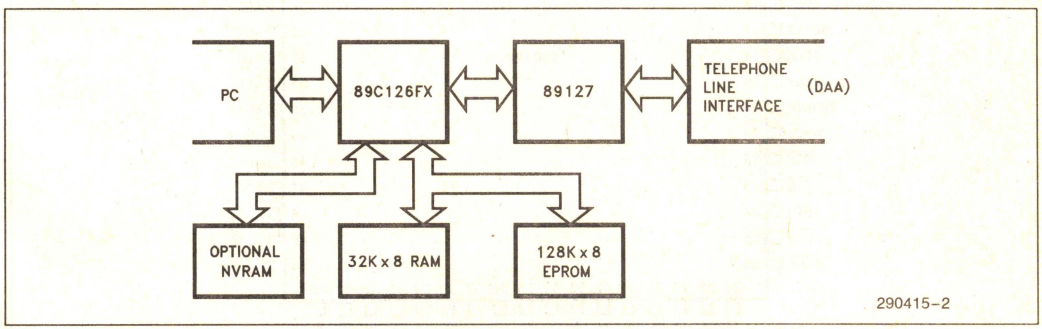


Figure 2. 89C124FX System Block Diagram

PACKAGING

The 89C124FX chipset is available in PLCC and QFP packaging. The 89127 is also available in PDIP packaging. Packages are shown from top view, looking down on component side of PC board. Refer to Intel Packaging handbook, order number 240800 for more details on packaging.

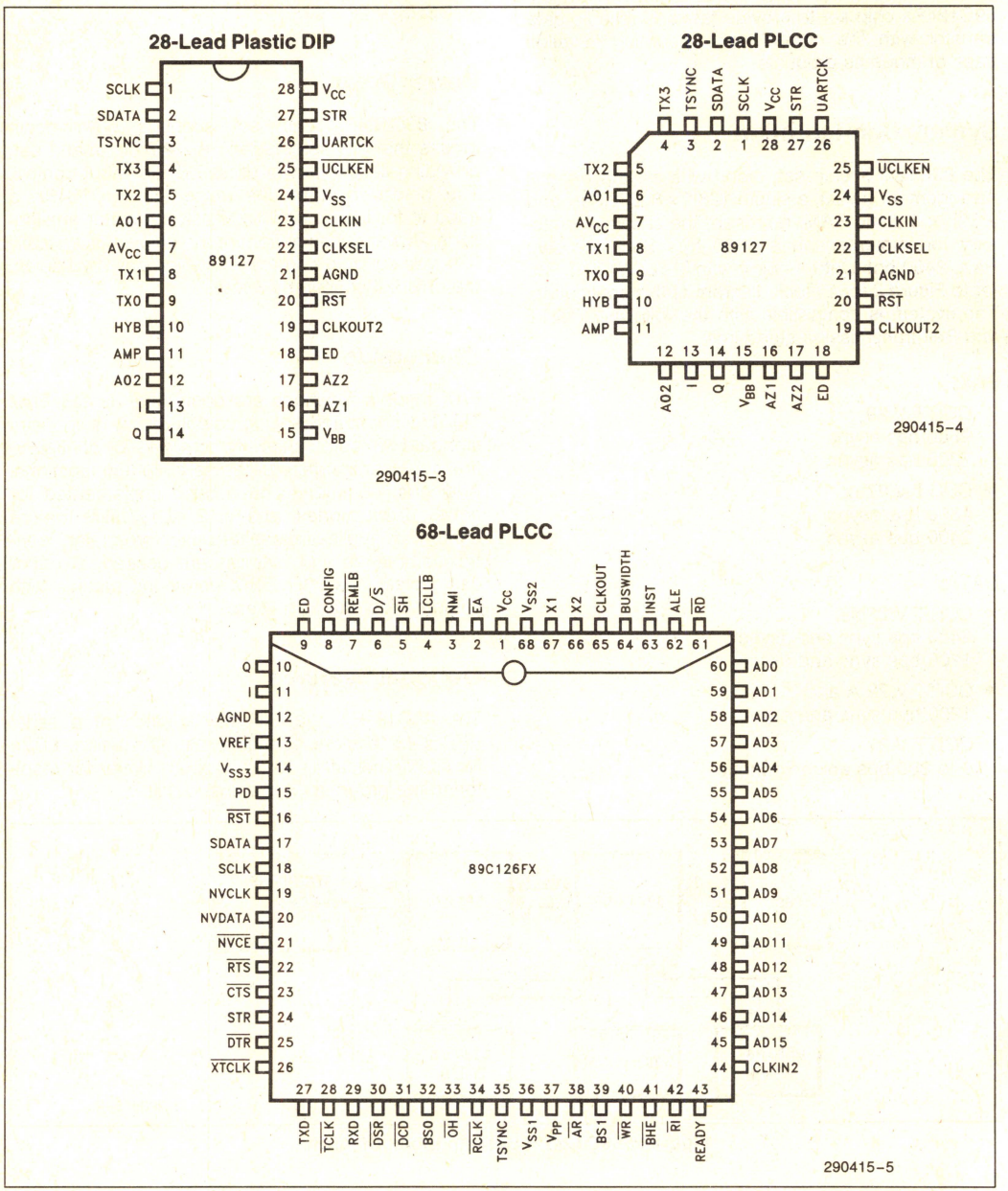
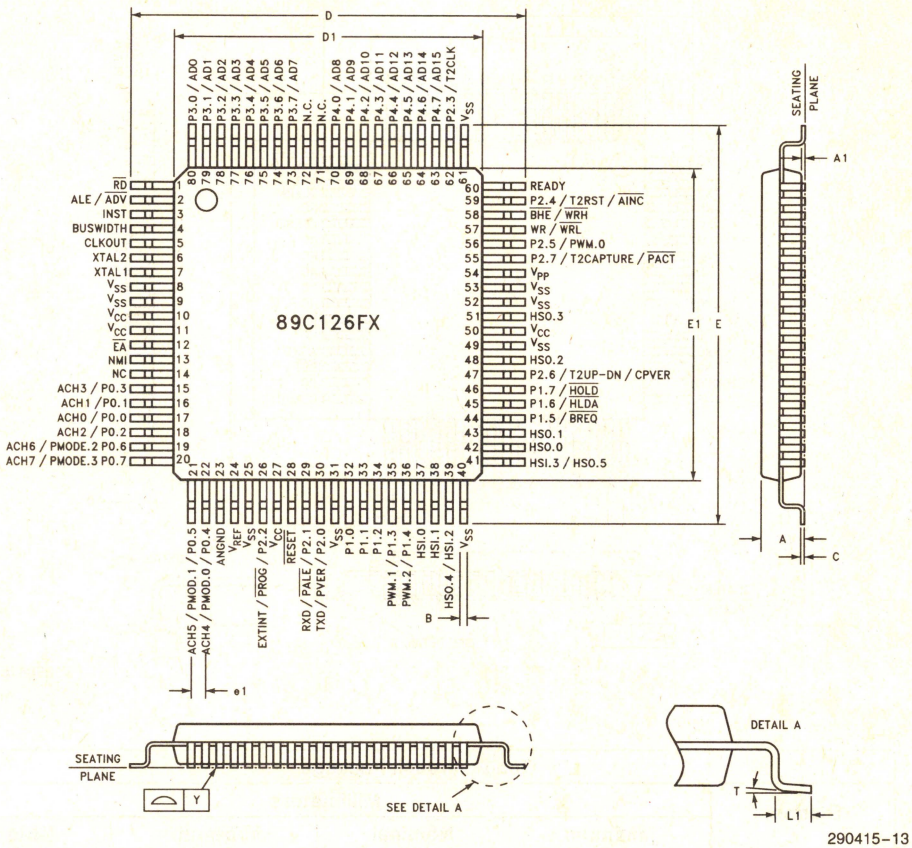


Figure 3. Device Packages

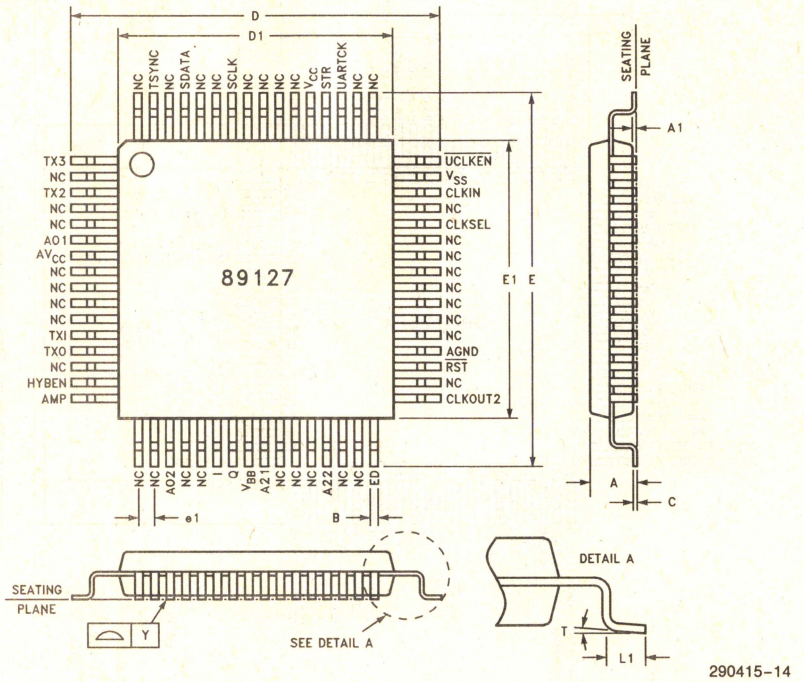
80-LEAD QFP



290415-13

Quad Flatpack Package				
Symbol	Millimeters			
	Minimum	Nominal	Maximum	Notes
A			1.66	
A_1	0.0			
B	0.14	0.20	0.26	
C	0.117	0.127	0.177	
D	13.7	14.0	14.3	
D_1		12.0		
E	13.7	14.0	14.3	
E_1		12.0		
e_1	0.40	0.50	0.60	
L_1	0.30	0.50	0.70	
N		80		Square
T	0.00		10.0	
Y			0.10	
ISSUE	EIAJ			

64-LEAD QFP



Quad Flatpack Package				
Symbol	Millimeters			
	Minimum	Nominal	Maximum	Notes
A			2.55	
A_1	0.0			
B	0.20	0.30	0.40	
C	0.10	0.15	0.20	
D	14.9	15.3	15.7	
D_1		12.0		
E	14.9	15.3	15.7	
E_1		12.0		
e_1	0.53	0.65	0.77	
L_1	0.65	0.85	1.05	
N		64		
T	0.00		10.0	
Y			0.10	
ISSUE	EIAJ			

CALL ESTABLISHMENT, TERMINATION AND RETRAIN (DATA MODEM)

The 89C124FX incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The chip set has a built-in auto-dialer, both DTMF and Pulse type. It can detect dial, busy, and ringback signals from the remote end, and will provide call progress messages to the user. The modem is also capable of re-dialing the last number dialed.

The modem, when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, and then transmit the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be set up by manual dialing. A transition from voice (i.e., for the purpose of manual dialing) to data mode can be done by the use of a mechanical switch (exclusion key) on the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests, originated by the remote modem, are of two types (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip set can also be configured to transmit "long-space" just before disconnection.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22bis to 212A), the Intel chip set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22bis standard, transparently, to 212A users. Similarly, a user with a 89C124FX based modem system can automatically call data bases with either 212A or V.22bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C124FX commands and registers that may be used while configuring the data/FAX modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered separately or in string fashion. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the "backspace" key (CNTRL-H) can be used to correct any error. Upper case or lower case characters can be used in the commands.

Table 1. Remote Modem Compatibility

Originating 89C124FX Modem		Answering Modem: Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89C124FX Modem		Originating Modem: Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

NOTE:
* These connection data rates are obtained when connecting 89C124FX based modems end to end. The same results may not be obtained when a 89C124FX based modem is connected to other modems.

Data Modem Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 300 and 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ;] @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code
%N	Maximum Line (DCE) Rate
&Cn	DCD Options
&Dn	DTR Options
&Fn	Fetch Factory Configuration Profile
&Gn	Guard Tone
&Jn	Telephone Jack Selection
&Ln	Leased/Dial-up Line Selection
&Mn	Async/Sync Mode Selection
&Pn	Make/Break Pulse Ratio
&Rn	RTS/CTS Options
&Sn	DSR Options
&Tn	Test Commands
&Wn	Write Configuration to Non Volatile Memory
&Xn	Sync Clock Source
&Yn	Default NVRAM Profile Select
&Zn	Store Telephone Number

EIA/TIA-578 FAX Command Set

+FCLASS= <value>	Service Class Selection
+FCLASS?	Read Current Service Class
+FCLASS=?	Read Service Class Capabilities
+FTS=<TIME>	Stop Transmission and Wait
+FRS=<TIME>	Wait for Silence
+FTM=<MOD>	Transmit Data
+FRM=<MOD>	Receive Data
+FTH=<MOD>	Transmit HDLC Data
+FRH=<MOD>	Receive HDLC Data
+FRM/H=?	Read Receive Speed Capabilities
+FTM/H=?	Read Transmit Speed Capabilities

V.42/42bis Feature Control Commands

−Jn	V.42 Detection Phase Control
"Hn	V.42bis Compression Control
"Nn	V.42bis Dictionary Size
"On	V.42bis Dictionary Sizing Length

MNP Feature Control Command Set

\An	Maximum MNP Block Size
%An	Set Auto-Reliable Fallback Character
\Bn	Transmit Break
\Cn	Set Auto-Reliable Buffer
%Cn	Set MNP Compression
\Gn	Set Modem Port Flow Control
\Jn	Bits per Second Rate Adjust
\Kn	Set Break Control
\Nn	Set Operating Mode
\O	Originate Reliable Link
\Qn	Set Serial Port Flow Control
\S	View Active Configuration
\Tn	Set Inactivity Timer
\U	Accept Reliable Link
\Vn	Modify Result Code Form
\Xn	Set XON/XOFF Pass-Through
\Y	Switch to Reliable Mode
\Z	Switch to Normal Mode

Power Down Commands

+En	Disable/Enable Power Down
+Tn	Time to Power Down

CONFIGURATION REGISTERS

The 89C124FX stores all the configuration information in a set of registers. Some registers are dedicated to a special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11 *	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register
S31 *	Bit Mapped Options Register
S37	Maximum Line (DCE) Rate
S100	Mean Error Monitor Register
S101	FAX Compromise Equalizer Control
S102	Force FAX Transmit and Receive Rates

NOTE:
* These S registers can be stored in the NVRAM.

DIALING

Dial modifiers are available for adding conditions to dialed phone numbers.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z0 = T 1 (602) 555-1212
Modem: OK

Result: Modem stores the Tone Dial (T) modifier and phone number T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS0
Modem: T16025551212

Result: Modem dials phone number and attempts to establish a connection.

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

POWER MANAGEMENT

The flexible power management controls allow for a variety of command and hardware driver options. The power-down sequence is initiated by placing a logic "low" on pin 15 ($\overline{PD}$) of the 89C126FX. The laptop or notebook can control the $\overline{PD}$ signal directly. If such a signal is unavailable, $\overline{PD}$ can be controlled by communications software via $\overline{DTR}$. Lack of data activity or an incoming ring signal can also be used to control $\overline{PD}$.

The 89C126FX reduces power consumption by turning off the oscillator. When online and connected to a remote modem, the power consumption for the 89C126FX is typically 530 mW. When the 89127 is not needed (e.g., on-hook, not connected to a remote modem) the 89C126FX places it in idle. In idle, the chip set power consumption is typically 365 mW. In powered down mode, the chip set typically consumes 7 mW. Memory-system power consumption can be minimized by chip selecting memory only when addressed.

APPLICATIONS OVERVIEW

A typical hardware configuration is illustrated in Figure 4 and consists of the following:

- 89C126FX with 21.600 MHz Crystal
- 89127 Analog Front End
- 1 128K x 8 120 ns EPROM (e.g., Intel 27C010-120)
- 1 32K x 8 120 ns SRAM (e.g. 51256-12)
- Bank Switching Logic
- 1K 93C46 Serial EEPROM (Optional)
- Power-Down Logic (Optional)
- Data Access Arrangement (DAA)
- UART (Internal Modem) or Serial Drivers (External Modem)

The DAA section shown in Figure 4 may be implemented using the suggested diagram in Figure 5. Figure 6 shows the use of the power-down feature.

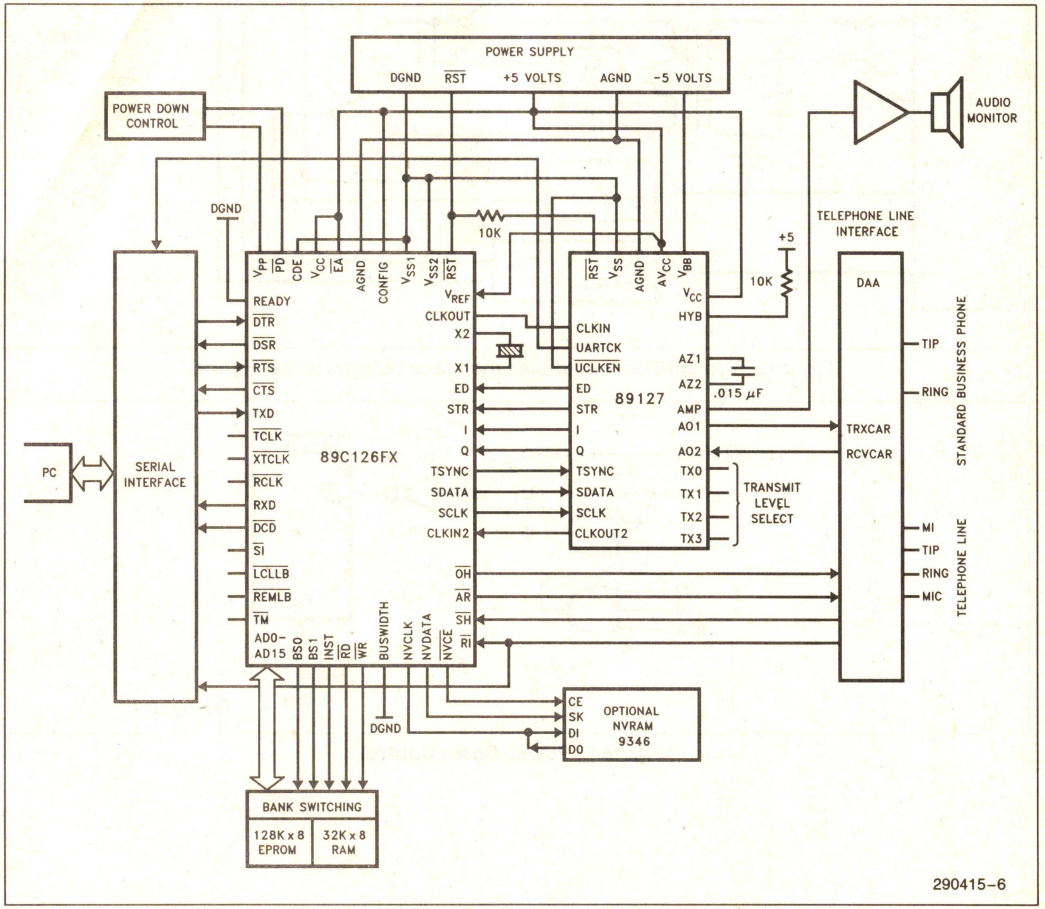


Figure 4. Typical Data FAX Modem

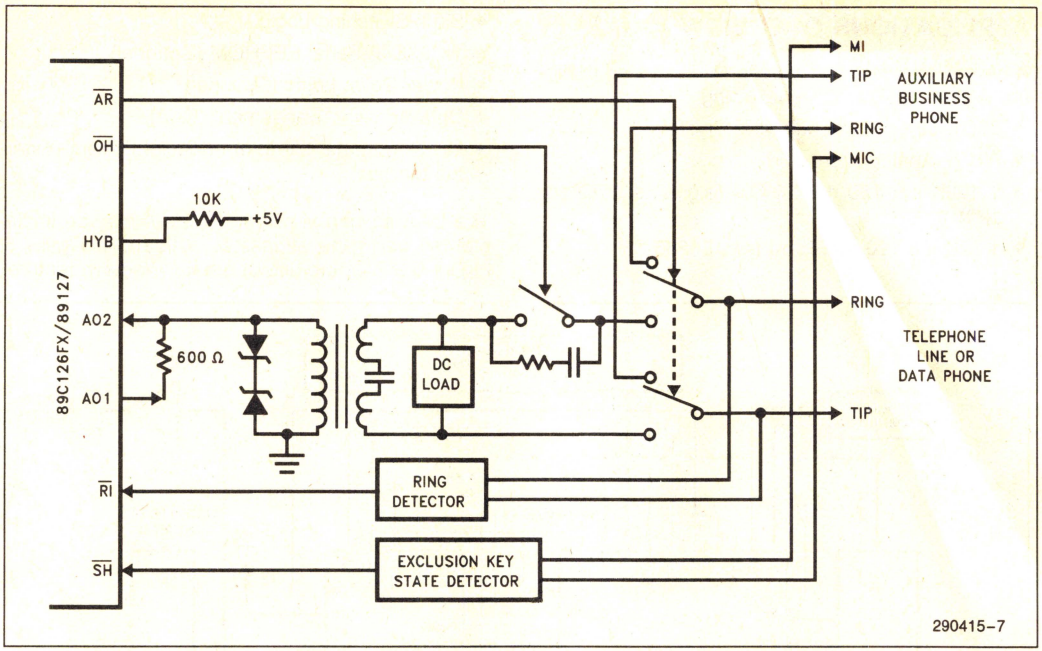


Figure 5. Typical Telephone Line Interface Using Internal Hybrid

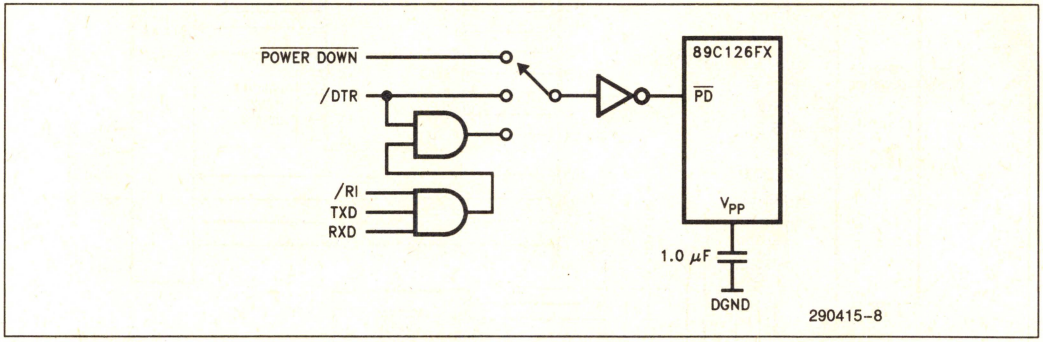


Figure 6. Power-Down Control

SYSTEM COMPATIBILITY SPECIFICATIONS

Specifications at DTE Interface

Parameter	Specification
Direct Mode Synchronous Asynchronous	 2400 bps ±0.01% V.22bis 1200 bps ±0.01% V.22 and BELL 212A 2400, 1200 bps, character async. 0 bps–300 bps anisochronous.
Buffered and Error Correction/Compression Command Modes	9600, 4800, 2400, 1200, 300 bps character asynchronous. (In online command mode, 110 bps and 300 bps only.)
FAX Mode	19,200 bps asynchronous only.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. (8, 9, 11 bits optional via software customization.)
Synchronous Timing Source	a) Internal, derived from the local oscillator (default). b) External, provided by DTE through $\overline{\text{XTCLK}}$. c) Slave, derived from the received clock.

Specifications at Telephone Line Interface

Parameter	Specification	
Telephone Line Interface	Two-wire full duplex over PSTN, or 4-wire leased lines (modem only). On-chip hybrid and billing delay timer.	
Modulation	V.29, QAM at 9600/7200 bps. V.27 ter, PSK at 4800/2400 bps. V.22bis, QAM at 2400 bps. V.22 and Bell 212A, PSK at 1200 bps. V.21 and Bell 103, FSK at 0–300 bps.	
Transmit Carrier Frequencies V.29 V.27ter V.22bis, V.22 Bell 212A	 Originate Answer	 1700 Hz ±1 Hz 1800 Hz ±1 Hz 1200 Hz ±.01% 2400 Hz ±.01%
Transmit Mark and Space Frequencies V.21 Bell 103	 Originate 'space' Originate 'mark' Answer 'space' Answer 'mark' Originate 'space' Originate 'mark' Answer 'space' Answer 'mark'	 1180 Hz ±0.2% 980 Hz ±.02% 1850 Hz ±0.2% 1650 Hz ±.02% 1070 Hz ±.02% 1270 Hz ±.02% 2020 Hz ±.02% 2225 Hz ±.02%

Specifications at Telephone Line Interface (Continued)

Parameter	Specification	
Received Carrier Frequency Tolerances		
V.29		1700 Hz ±7 Hz
V.27ter		1800 Hz ±7 Hz
V.22bis, V.22, Bell 212A	Originate	2400 Hz ±7 Hz
	Answer	1200 Hz ±7 Hz
Received Mark and Space Frequency Tolerances		
V.21	Originate 'space'	1850 Hz ±12 Hz
	Originate 'mark'	1650 Hz ±12 Hz
	Answer 'space'	1180 Hz ±12 Hz
	Answer 'mark'	980 Hz ±12 Hz
Bell 103	Originate 'space'	2020 Hz ±12 Hz
	Originate 'mark'	2225 Hz ±12 Hz
	Answer 'space'	1070 Hz ±12 Hz
	Answer 'mark'	1270 Hz ±12 Hz
Typical Energy Detect Sensitivity	> −43 dBm ED is ON. < −48 dBm ED is OFF. Signal measured at AO2.	
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.	
Line Equalization	Automatic Adaptive Equalizer for PSK/QAM receive.	

Data Modem Diagnostics

The diagnostics in this section apply only to Data Modem, and not FAX.

Parameter	Specification
Diagnostics Available	Local Analog Loopback. Local Digital Loopback. Remote Digital Loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeroes' and error detector, to be used with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	Rx Level (dBm)	Answer (dB)	Originate (dB)
V.22bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

— Receive Signal (Rx) measured at A02 (transmit level set at −9 dBm)

— Unconditioned 3002 Line

— 3 KHz Flat-Band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10/20		pps	Software Controlled
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	 referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89C126FX OVERVIEW

The 89C126FX processor performs data manipulation, signal processing and user interface functions. It requires a single 128K x 8 ROM and 32K x 8 RAM to execute standard, and/or custom code to perform the V.42/42bis, MNP4/5 and FAX protocol functions. A bank switching scheme is used to accommodate the full range of ROM and RAM addresses. Addresses are decoded using the INST, BS0, and BS1 signals. A block diagram of the 89C126FX is provided in Figure 7.

89C126FX contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. A UART or USART may be used to transfer data to and from a microcomputer bus. The 89C126FX supports the industry standard AT command set for data modem and EIA/TIA-578 command set for FAX modem functions.

During transmit operation, the 89C126FX synthesizes DTMF tones, 300 BPS FSK signal, and the FAX 9600/7200/4800/2400 bps signals and transmits them to the 89127 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C126FX transmits digitized phase and amplitude samples to 89127 over the high speed serial link.

In data modem receive operation, the information is received by the 89C126FX from the 89127 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C126FX. DSP algorithms are utilized to implement adaptive equalization, amplitude distortion and gain adjustments, and demodulation. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

In FAX receive operation, the information is received by the 89C126FX from the 89127 as a filtered and sampled version of the signal on the phone line. The analog signal is digitized by the A/D converter resident on the 89C126FX. DSP algorithms are utilized to implement bandpass filtering, adaptive equalization, and demodulation. Following demodulation, the data is unscrambled.

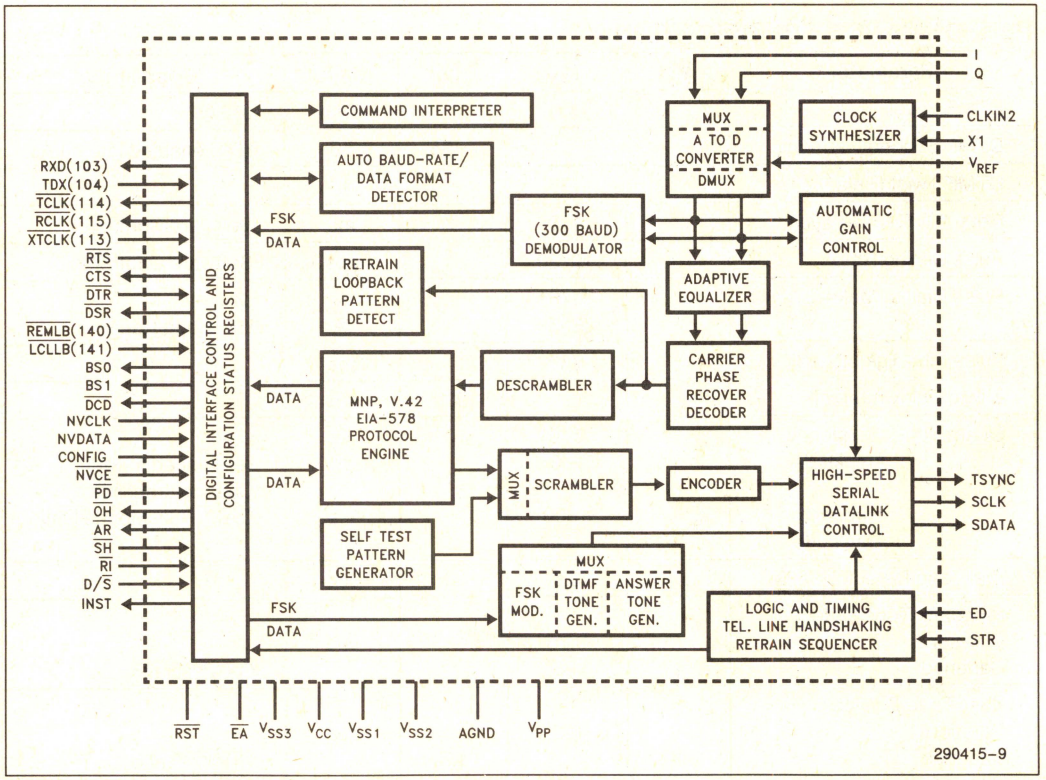


Figure 7. 89C126FX Block Diagram

89C126FX PINOUT

Symbol	Function (89C126FX)	Direction	Pin No.
X1	Crystal Input(2)	In	67
X2	Crystal Output	Out	66
CLKIN2	432 KHz Input from 89127	In	44
CLKOUT	Clock Output to 89127	Out	65
$\overline{RST}$	Chip Reset (Active Low)	In	16
I	In-Phase Received Signal	In	11
Q	Quadrature-Phase Received Signal	In	10
STR	Symbol Timing from 89127	In	24
ED	Energy Detect Input	In	9
TSYNC	Transmitter Sync Pulse to 89127	Out	35
SDATA	Serial Data to 89127	Out	17
SCLK	Serial Clock to 89127	Out	18
$\overline{OH}$	Off-Hook Control to DAA	Out	33
$\overline{SH}$	Switch-Hook from Dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay Control to DAA	Out	38
NVDATA	NVRAM Data I/O(1)	I/O	20
NVCLK	NVRAM Clock	Out	19
$\overline{NVCE}$	NVRAM Chip Enable(1)	Out	21
$\overline{PD}$	Power-Down Control	In	15
D/$\overline{S}$	Dumb/$\overline{Smart}$ Mode Select	In	6
CONFIG	Reserved for Future Use (Must be Connected to V_{CC})	In	8
BS0	Bank Select 0(3)	Out	32
BS1	Bank Select 1(3)	Out	39
TXD	Transmitted Data from DTE	In	27
RXD	Received Data to DTE	Out	29
$\overline{RTS}$	Request to Send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received Clock to DTE	Out	34
$\overline{TCLK}$	Transmit Clock to DTE	Out	28
$\overline{XTCLK}$	External Timing Clock from DTE	In	26
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive Power Supply (+5V)	+5V	1
V_{REF}	A/D Converter Reference	+5V	13
V_{SS1}	Digital Ground	GND	36
V_{SS2}	Digital Ground	GND	68
V_{SS3}	Digital Ground(4)	GND	14
AGND	Analog Ground	AGND	12
V_{PP}	Timing Pin for Return from Power-Down	In	37

89C126FX PINOUT

Symbol	Function (89C126FX)	Direction	Pin No.
$\overline{EA}$	External Memory Enable	In	2
AD0–AD15	External Memory Access Address/Data	I/O	60–45
$\overline{AA}$	Auto Answer(5)	Out	60
$\overline{JS}$	Jack Select(5)	Out	59
$\overline{CD}$	Carrier Detect Indicator(5)	Out	58
$\overline{MR}$	Modem Ready Indicator(5)	Out	57
$\overline{REL}$	MNP Reliable Link Active(5)	Out	56
$\overline{COMP}$	Compression Active V.42bis or MNP 5(5)	Out	55
$\overline{ERR}$	Error Detected by LAPM or MNP(5)	Out	54
$\overline{LAPM}$	LAPM Reliable Link Active(5)	Out	53
$\overline{SI}$	Speed Indicator to DTE(5)	Out	60
$\overline{FAX}$	FAX Protocol is Active(5)	Out	59
TM	Test Mode Indicator(5)	Out	58
NMI	Non-Maskable Interrupt	In	3
BUSWIDTH	Bus Width	In	64
INST	External Memory Instruction Fetch	Out	63
ALE	Address Latch Enable	Out	62
$\overline{RD}$	External Memory Read	Out	61
READY	External Memory Ready	In	43
$\overline{BHE}$	External Memory Bus High Enable	Out	41
$\overline{WR}$	External Memory Write	Out	40

NOTES:
1. $\overline{NVCE}$, NVDATA and NVCLK are known as S/A, TCL1, and TCL0, respectively on the 89C024FT. These pins have the same functionality; only the names are different.
2. X1 is known as CLKIN on the 89C024FT, only the naming is different.
3. BS0 and BS1 are known as $\overline{SI}$ and $\overline{TM}$ respectively on the 89C024FT. Their functionality is different. $\overline{SI}$ and $\overline{TM}$ are memory mapped outputs of the 89C124FX.
4. V_{SS3} is known as CDE on the 89C024FT, only the naming is different.
5. These signals are memory mapped, and must be latched externally.

89C126FX PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89C126FX samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89C126FX as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. A logic 'high' is mark. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

$\overline{PD}$

Power-down control. A low on this input pin, in conjunction with the +En and +Tn commands, will cause the modem to go into a power-down mode.

V_{PP}

Timing pin for return from power-down. Connect a 1.0 μF capacitor between V_{PP} and V_{SS} if the power-

down option is used. This capacitor causes an internal timing circuit to give the oscillator time to stabilize before turning on internal clocks. This pin may be left floating or connected through a 1.0 μF capacitor to V_{SS} if power-down mode is not required.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation, low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

A low indicates modem is off-hook, is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a low-to-high transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A low-to-high transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

BS0, BS1

Bank Select Pins. These outputs are used by the bank switching logic to generate the MSB address lines for the external ROM.

NVCLK, NVDATA, $\overline{NVCE}$

These pins are used as the serial clock and data for interface to an NVRAM. NVCLK is used to output a clock and serial data is transferred in on NVDATA. $\overline{NVCE}$ is a chip enable for the NVRAM.

$\overline{AR}$

This Auxiliary Relay control is for switching a relay for voice or data calls. High is voice, low is data.

$\overline{RI}$

A low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high indicates an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins sets the modem to the local digital loopback.

$\overline{REMLB}$

A low on this pin initiates a remote loopback condition.

$\overline{CD}$

A low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test mode is active.

$\overline{REL}$

A low indicates that an MNP reliable link has been established.

$\overline{COMP}$

A low indicates that data compression is in operation (V.42bis or MNP Class 5).

$\overline{LAPM}$

A low indicates that a LAPM reliable link has been established.

$\overline{ERR}$

Goes low for 1 second whenever a reliable connection detects an error.

D/$\overline{S}$

A low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89127 AV_{CC}.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 Bell) or range of rates. High selects the Low rate or range of rates.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory. This pin must be tied high.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

BUSWIDTH

When high, external memory accesses are 16 bits wide. When low, external memory accesses are 8 bits wide. This pin must be tied low.

READY

When high, no wait states are inserted in external memory accesses. When low, two wait states are inserted in each external memory access.

INST

Output high during an external memory read indicates the read is an instruction fetch. INST is activated only during external memory accesses and output low for data fetch. INST along with AD15 are used to decode the overlapping external ROM and RAM.

$\overline{TM}$

Low indicates maintenance condition in the modem.

$\overline{FAX}$

Low indicates that the modem is off hook in the FAX mode.

89C126FX
Absolute Maximum Ratings*

Ambient Temperature
Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin to V_{SS} . . . . . −0.5V to +7.0V
Power Dissipation 1.5W

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

Operating Conditions

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
f_{OSC}	Oscillator Frequency	21.5978	21.6022	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

D.C. Characteristics (Over specified operating conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{\text{RESET}}$	150		mV	V_{CC} = 5.0V
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA
V_{OH2}	Output High Voltage in RESET on P2.0 (Note 2)	2.0		V	I_{OH} = −0.8 mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	μA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		±3	μA	0 < V_{IN} < V_{REF}

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.

D.C. Characteristics (Over specified operating conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	V_{IN} = 0.45V
I_{IL1}	AD Bus in Reset			−70	μA	V_{IN} = 0.45V
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 21.6 MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5V
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current		15	TBD	μA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5V
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	V_{CC} = 5.5V, V_{IN} = 4.0V
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

A.C. Characteristics

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} = 21.6 MHz

The system must meet these specifications to work with the 89C124FX:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 68$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 68$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC}$ * N, where N = number of wait states.

The 89C124FX will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$			MHz	
T_{OSC}	$1/F_{XTAL}$			ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns	
T_{CLCL}	CLKOUT Cycle Time	$2T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	$4T_{OSC}$		ns	(Note 3)
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 15$			
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 30$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$		ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$			(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 20$		ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 25$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	$T_{OSC} - 30$		ns	(Note 2)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	$T_{OSC} - 30$		ns	(Note 2)

NOTES:
1. Assuming back-to-back bus cycles.
2. 8-Bit bus only.
3. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

Waveforms

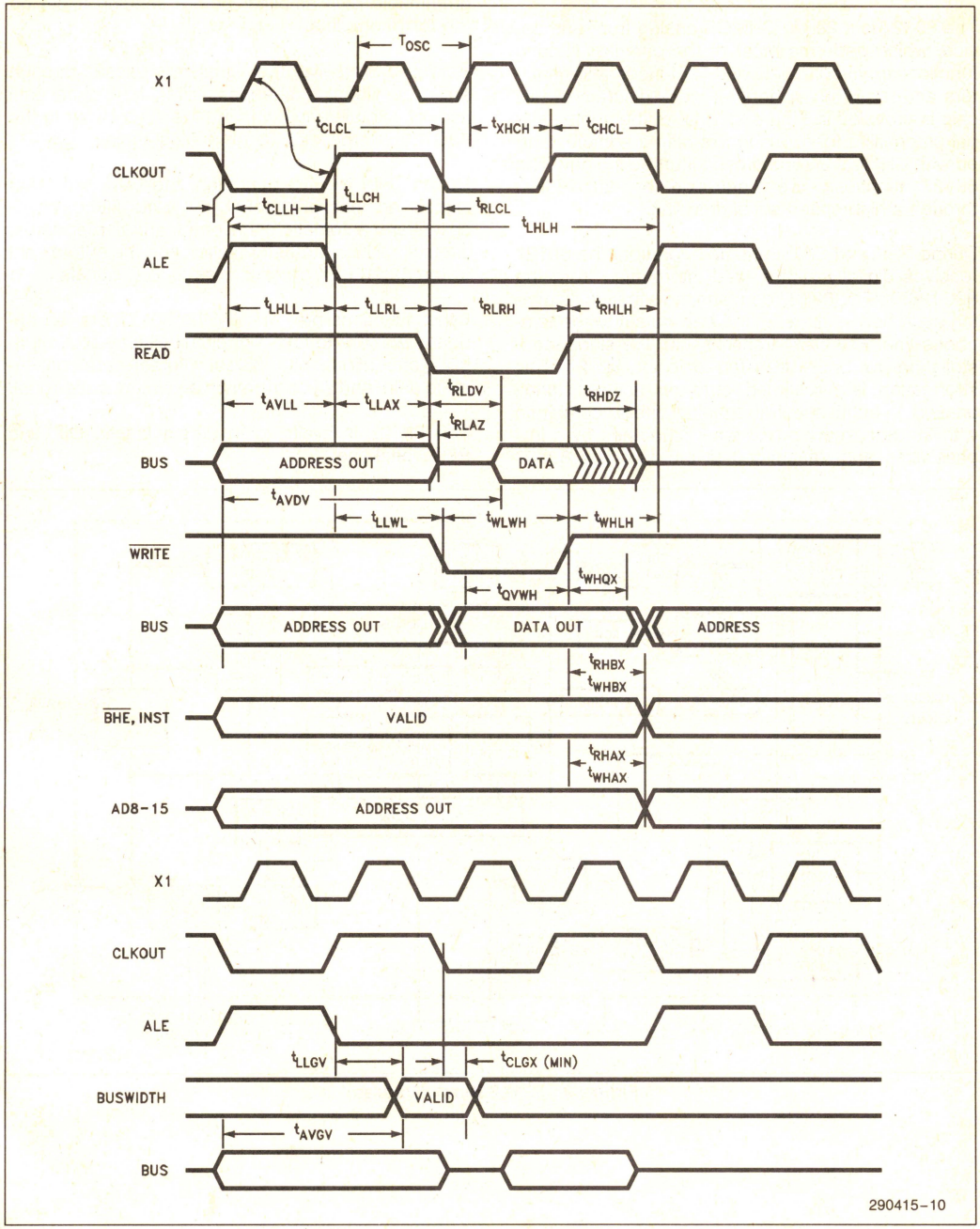


Figure 8. Bus Signal Timings

89127 OVERVIEW

The 89127 is a 28-pin CHMOS analog front end device, which performs most of the complex filtering functions required in data and FAX modem transmitters and receivers. A general block diagram of this chip is provided in Figure 9. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89127 functions are controlled by 89C126FX, through a high speed serial data link.

During FSK and FAX transmit operation, the 89127 receives digitally synthesized information from the 89C126FX. The 89127 converts the signal to its analog equivalents, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89127. This information is modulated onto an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. The 89127 adjusts the signal gain through an on-board programmable gain amplifier before sending it out on the telephone line.

During FAX receive, the signals are passed through anti-alias filters, a bandpass filter, automatic gain control, sample and hold, and the output sent to the 89C126FX processor as an analog signal.

During Data receive operation, the FSK and QAM signals are passed through anti-alias filters, band-split filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C126FX processor as analog signals.

Other functions provided by the 89127 are: an on-board two-wire to four-wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89127 is available in 28-pin plastic DIP and PLCC packages.

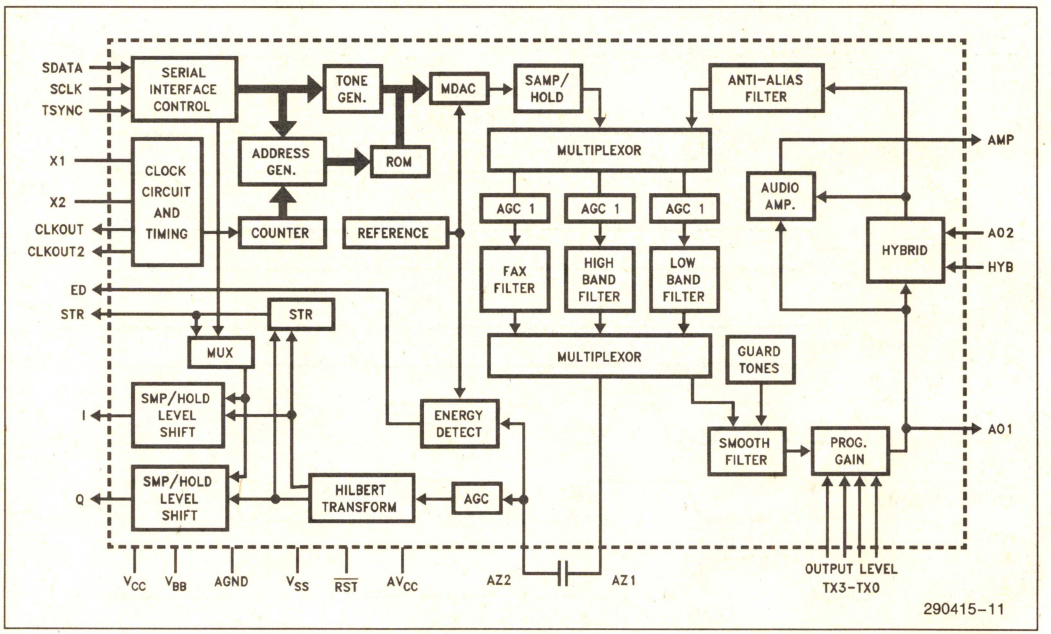


Figure 9. 89127 Block Diagram

89127 PINOUT

Symbol	Function (89127)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
CLKIN	Clock Input(1)	In	23
CLKSEL	Clock Select(2)	In	22
$\overline{\text{UCLKEN}}$	UART Clock Enable(3)	In	25
UARTCK	UART Clock(4)	Out	26
CLKOUT2	432 KHz Clock Output to 89C126FX	Out	19
$\overline{\text{RST}}$	Chip Reset	In	20
HYB	Enable On-Chip Hybrid	In	10
AZ1	Auto-Zero Capacitor	Out	16
AZ2	Auto-Zero Capacitor	In	17
SDATA	Serial Data from 89C126FX	In	2
SCLK	Serial Clock from 89C126FX	In	1
TSYNC	Transmitter Sync from 89C126FX	In	3
STR	Symbol Timing to 89C126FX	Out	27
ED	Receiver Energy Detect to 89C126FX	Out	18
I	In-Phase Received Signal to 89C126FX	Out	13
Q	Quadrature-Phase Received Signal to 89C126FX	Out	14
AO1	Transmitter Output	Out	6
AO2	Receiver Input	In	12
AMP	Output to Monitor Speaker	Out	11
TX0	Transmitter Level Control (LSB)	In	9
TX1	Transmitter Level Control	In	8
TX2	Transmitter Level Control	In	5
TX3	Transmitter Level Control (MSB)	In	4

NOTES:
1. CLKIN is known as X1 on the 89C024FT, only the naming is different.
2. This pin is a "no connect" on 89C024FT. This is an added function.
3. $\overline{\text{UCLKEN}}$ is known as X2 on 89C024FT. Their functionality is different.
4. UARTCK is known as CLOCKOUT on 89C024FT. Their functionality is different.

89127 Pinout Description

CLKIN

Clock Input from 89C126FX.

CLKSEL

Clock Select Pin. GND selects 10.8 MHz clock, V_{BB} selects 6.48 MHz clock.

$\overline{\text{UCLKEN}}$

Enables UARTCK when tied low (V_{SS}). If this pin is pulled up, UARTCK is disabled.

UARTCK

Acts as the clock for a UART. Eliminates the need for a crystal on internal Data/FAX modem designs.

CLKOUT2

A 432 KHz clocking signal output that goes to the 89C126FX.

$\overline{\text{RST}}$

Active low reset signal. Connect to the controller's $\overline{\text{RST}}$ pin.

HYB

Hybrid Enable. A logic high on this pin enables the on-chip hybrid for two-wire telephone line communication. This input, if tied high, must be tied high through a 10K resistor. If HYB is enabled, a line impedance matching network must be connected between AO1 and AO2. If HYB is disabled, and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AZ1, AZ2

Connections for Auto Zeroing Capacitor.

SDATA, SCLK, TSYNC

These pins constitute the serial link used to transmit data from the 89C126FX to the 89127.

ABSOLUTE MAXIMUM RATINGS(2)

Temperature Under Bias ..... 0 to +70° C

Storage Temperature ..... −40 to +125° C

All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V

All Input and Output Voltages with Respect to V_{CC} & AV_{CC} ..... −13.0V to 0.3V

Power Dissipation 1.35W

Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

AMP

A speaker driver can be connected to this pin, allowing monitoring of call progress tones and operation of the line.

TX0-3

These four pins control the transmitted signal level.

NOTES:

1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0-TX3 only.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{BB}	Analog Supply Voltage	−4.75	−5.25	V

POWER DISSIPATION Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ±5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$Alcc_1$	AV_{CC} Operating Current		16.5	25	mA
Icc_1	V_{CC} Operating Current		5.5	7.2	mA
Ibb_1	V_{BB} Operating Current		−16.5	−25.2	mA
$Alcc_s$	AV_{CC} Standby Current		0.2	1.2	mA
Icc_s	V_{CC} Standby Current		5.5	7.2	mA
Ibb_s	V_{BB} Standby Current		−0.7	−2.4	mA
$Alcc_p$	AV_{CC} Power-Down Current		110		μA
Icc_p	V_{CC} Power-Down Current		495		μA
Ibb_p	V_{BB} Power-Down Current		495		μA
Pdo	Operating Power Dissipation		193	300	mW
Pds	Standby Power Dissipation		33	60	mW
Pd_p	Power Down Power Dissipation		7		mW

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C126FX power supply. Typical Values are for T_A = 25°C and nominal power supply values. V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C126FX V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: UARTCK

Symbol	Parameter	Min	Max	Units	Test Conditions
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.0	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50μa, 1 TTL load
Vcol	UARTCK Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	UARTCK High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

A.C. CHARACTERISTICS

(T_A = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal Level			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V<Vin<+2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20%
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

CRYSTAL REQUIREMENTS

Parameter	Min	Typ	Max	Units
Frequency Accuracy (0°C–70°C)	−0.0025%	21.600	+0.0025%	MHz
Rx		10	16	Ω
Cx		0.024		pF
Co	5.1	5.6	6.1	pF
Cp		23		pF

NOTES:
1. Crystal Type: Parallel Resonant
2. Crystal manufacturers usually specify the accuracy of a parallel resonant circuit at a given "load capacitance", specified here as Cp, which includes the combination of all capacitances seen at the pins of the crystal. This includes CI, IC pin capacitances, and layout related trace capacitances.
3. Crystal accuracy requirements can be relaxed if layout parasitic capacitances are appropriately considered in the crystal selection.
4. Total capacitance attached to the X1 and X2 pins should not exceed 51 pF each unless Rx Max is decreased.

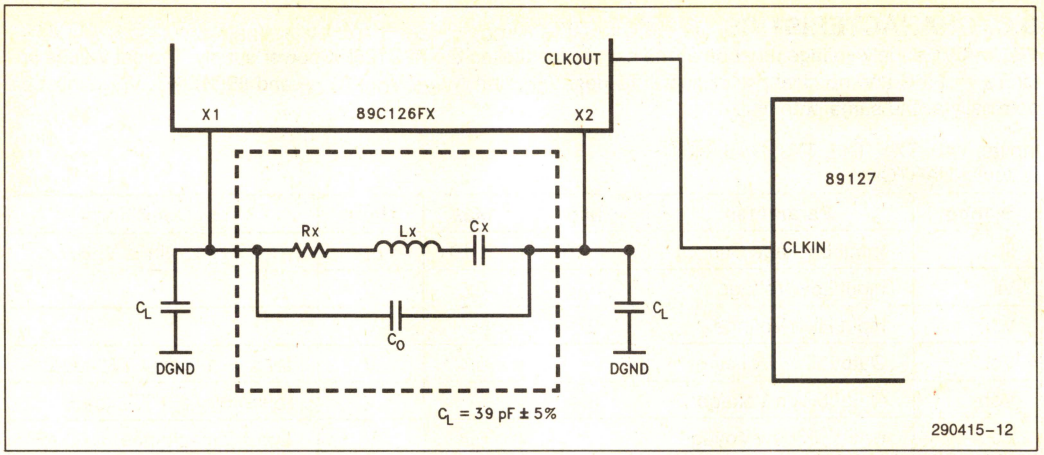


Figure 10. Crystal Equivalent Circuit

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 Ohms kOhms	
Load Capacitance AMP			100	pF	
Audio Amp Gain AO1 to Amp		−9 −18 −26 −70		dB dB dB dB	Max Mid Min Off (Software Selectable)
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −60		dB dB dB dB	Max Mid Min Off (Software Selectable)

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

SCHEMATICS AND PARTS LIST

The schematics and parts list are for an external data/fax modem design. By adding a UART, the 89C124FX may be used for internal card modem designs. For a schematic of a UART design to interface the 89C124FX to the ISA bus, refer to the Intel Modem Reference Manual, Order Number 296235.

MEMORY ADDRESSING LOGIC

The memory addressing "glue" logic may be implemented using discrete logic gates as in the schematics, or using a PLD (Programmable Logic Device). The equations for using a PLD are as follows:

RAM

$$\overline{CS1} = \overline{AD15} + INST$$

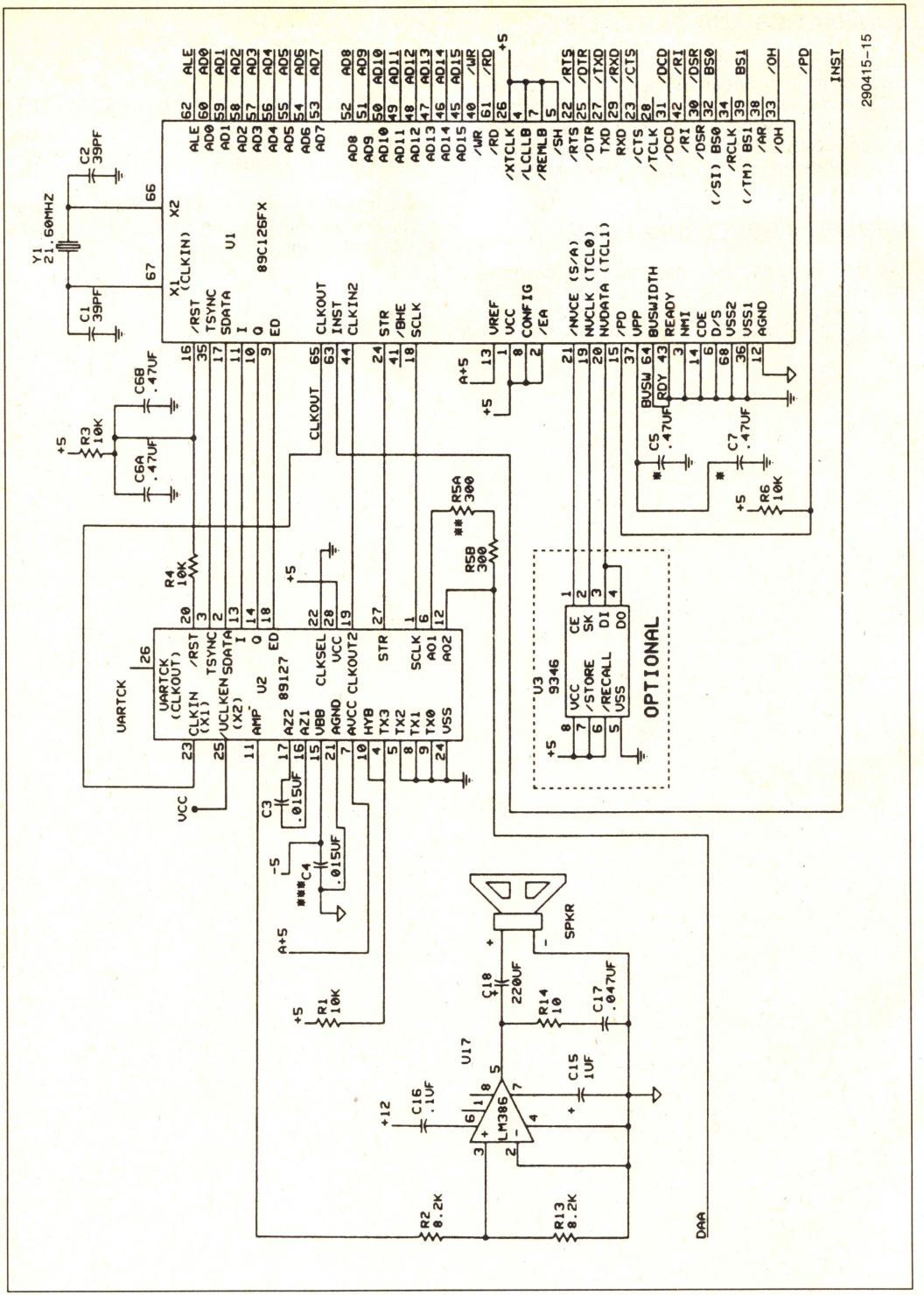
ROM

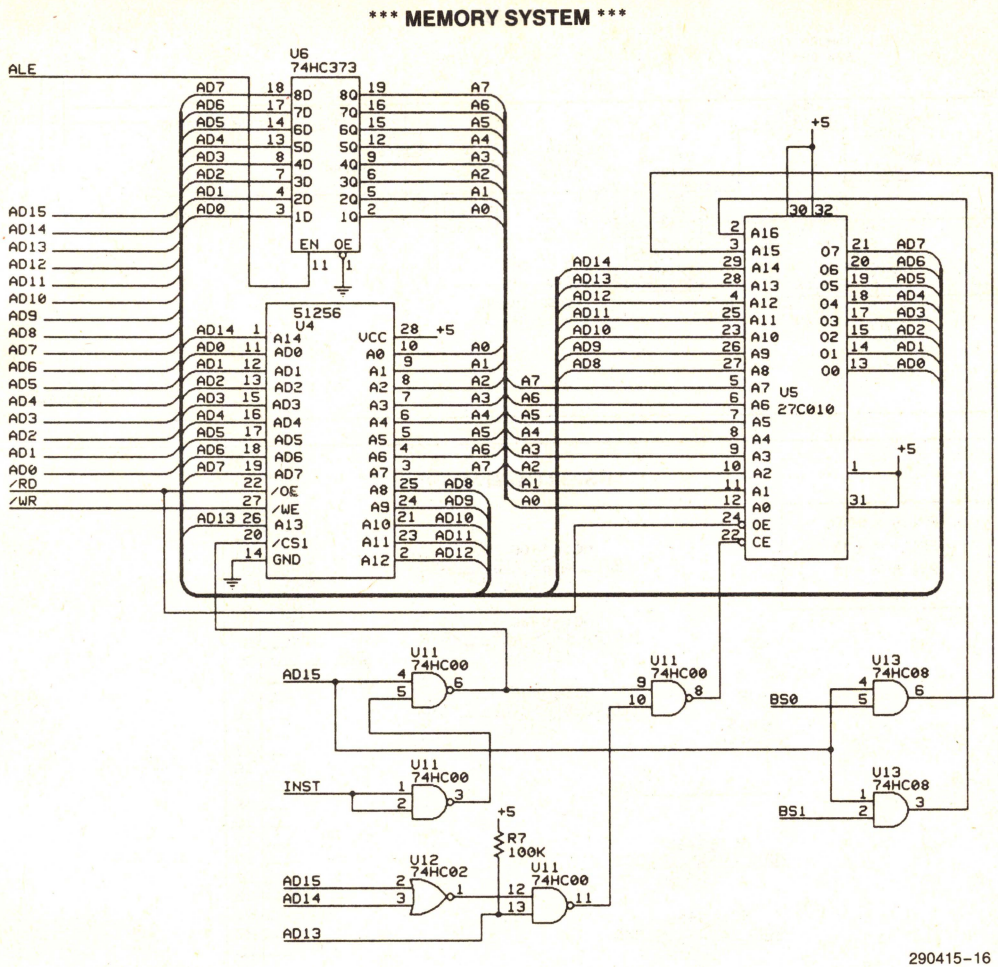
$$\overline{CE} = AD15 \bullet \overline{INST} + AD13 \bullet \overline{AD14} \bullet \overline{AD15}$$

$$A15 = BS0 \bullet AD15$$

$$A16 = BS1 \bullet AD16$$

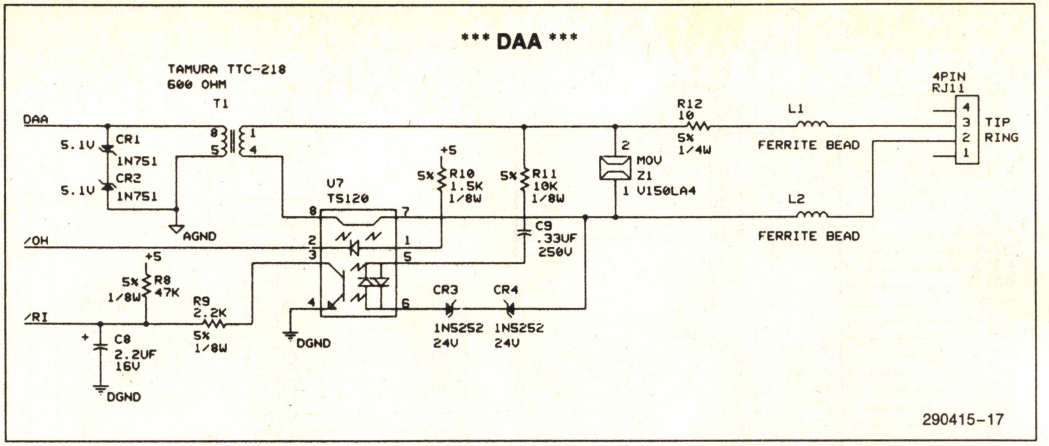
The term AD13 • $\overline{AD14}$ • $\overline{AD15}$ in the $\overline{CE}$ equation disables ROM during internal ROM accesses, and is an optional means for saving power.

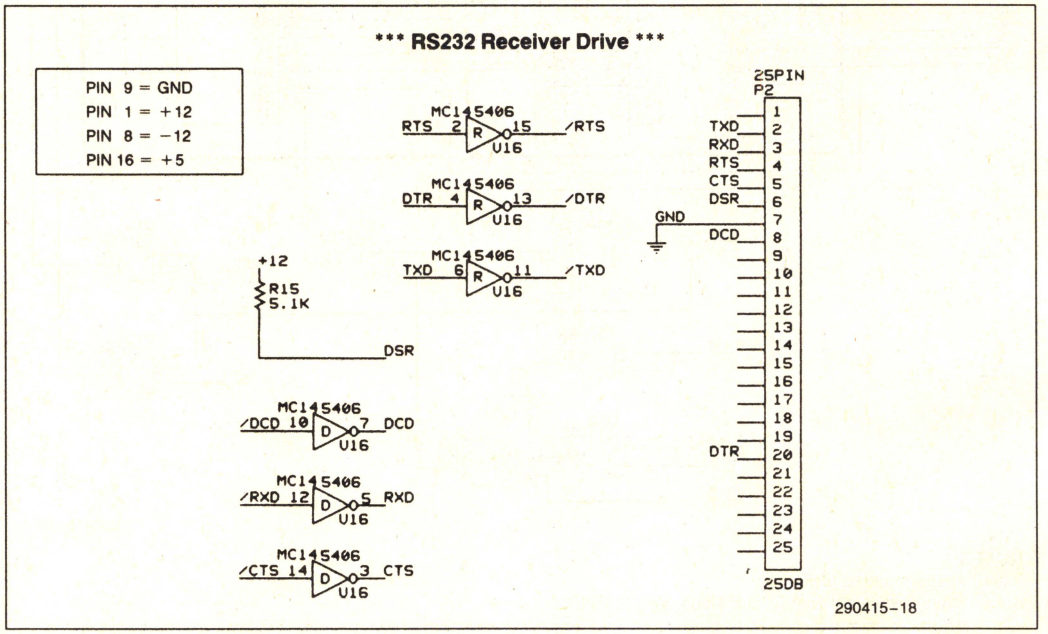

290415-15
OPTIONAL
DAA
SPKR
INST
PD
Y1 21.60MHZ
C1 39PF
C2 39PF
X1 (CLKIN)
X2
U1 89C125FX
/RST
TSYNC
SDATA
I
O
ED
CLKOUT
INST
CLKIN2
STR
/BHE
SCLK
VREF
VCC
CONFIG
/EA
/XTCLK
/LCLLB
/REMLB
/SH
/RTS
/DTR
/TXD
RXD
/CTS
/TCLK
/DCD
/RI
/DSR
(/SI) BS0
/RCLK
(/TM) BS1
/AR
/OH
ALE
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
/WR
/RD
/NVCE (S/A)
NVCLK (TCL0)
NVDATA (TCL1)
/PD
VPP
BUSWIDTH
READY
NMI
CDE
D/S
VSS2
VSS1
AGND
BUSW
RDY
C6A .47UF
C6B .47UF
R3 10K
R4 10K
C3 .015UF
C4 .015UF
C5 .47UF
C7 .47UF
R6 10K
R5A 300
R5B 300
U2 89127
UARTCK (CLKOUT)
CLKIN (X1)
/UCLKEN (X2)
AMP
AZ2
AZ1
VBB
AGND
AVCC
HYB
TX3
TX2
TX1
TX0
VSS
CLKSEL
VCC
CLKOUT2
STR
SCLK
AO1
AO2
U3 9346
VCC
/STORE
/RECALL
VSS
CE
SK
DI
DO
R1 10K
C10 220UF
R14 10
C17 .047UF
U17 LM386
C15 1UF
C16 .1UF
R2 8.2K
R13 8.2K
+5
+12
A+5
-5
VCC

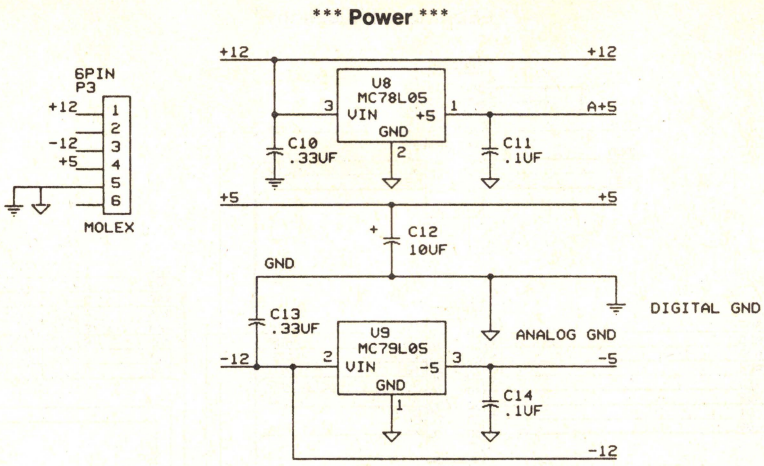


290415-16

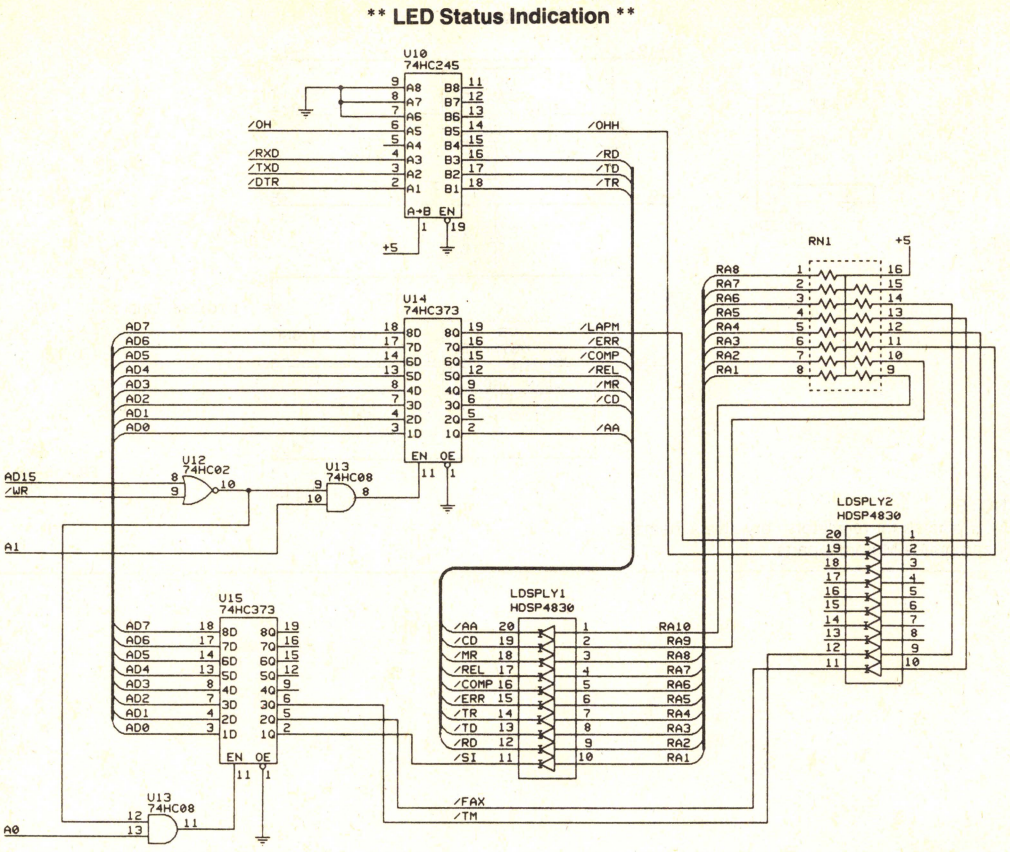
NOTES:
Tie all spare inputs to GND.
All IC's to be bypassed with 0.1 μF Caps, V_{CC} to GND.


*** DAA ***
TAMURA TTC-218
600 OHM
T1
DAA
5.1V
CR1
1N751
CR2
5.1V
1N751
AGND
/OH
+5
5%
R8
1/8W
47K
/RI
R9
2.2K
5%
1/8W
C8
2.2UF
16V
DGND
U7
TS120
+5
5%
R10
1.5K
1/8W
5%
R11
10K
1/8W
C9
.33UF
250V
CR3
CR4
1N5252
24V
1N5252
24V
DGND
R12
10
5%
1/4W
MOV
Z1
1 V150LA4
L1
FERRITE BEAD
L2
FERRITE BEAD
4PIN
RJ11
TIP
RING
290415-17


*** RS232 Receiver Drive ***
PIN 9 = GND
PIN 1 = +12
PIN 8 = −12
PIN 16 = +5
MC145406
RTS 2
/RTS
U16
MC145406
DTR 4
/DTR
U16
MC145406
TXD 6
/TXD
U16
+12
R15
5.1K
DSR
MC145406
/DCD 10
DCD
U16
MC145406
/RXD 12
RXD
U16
MC145406
/CTS 14
CTS
U16
25PIN
P2
TXD
RXD
RTS
CTS
DSR
GND
DCD
DTR
25DB
290415-18



NOTE:
Mfgr pinouts for regulators vary, this schematic incorporates Motorola parts.



NOTE:
Tie unused inputs to GND.

89C124FX External Modem Parts List

Part	Description
U1	Intel 89C126FX Microcontroller
U2	Intel 89127 Analog Front End
U3	93C46 EEPROM 1024-Bit (Optional)
U4	51256 32K x 8 SRAM 120 ns
U5	27C010 128K x 8 ROM 120 ns
U6	74HC373 Octal Transparent Latch
U7	Theta J TS120 Analog Opto Relay
U8	78L05A +5V Regulator
U9	79L05A −5V Regulator
U10	74HC245 Octal Bus Transceiver
U11	74HC00 Quad 2 Input NAND
U12	74HC02 Quad 2 Input NOR
U13	74HC08 Quad 2 Input AND
U14, U15	74HC373 Octal Transparent Latch
U16	MC145406 RS-232 Receiver Driver
C1, C2	39 pF ±5%
C3, C4	0.015 μF
C5, C6A, C6B, C7	0.47 μF
C8	2.2 μF 16V
C9	0.33 μF, 250V. MetalPoly
C10, C13	0.33 μF
C11, C14	0.10 μF
CR1, CR2	1N751A Zener Diode
CR3, CR4	1N5252B Zener Diode
L1, L2	3 Turn Ferrite Bead Inductor
R1, R3, R4, R6, R11	10K 1/8 W
R5A, R5B	300Ω 1/8 Watt 5%
R8	47K, 1/8 W, 5%
R9	2.2K, 1/8 W, 5%
R10	1.5K, 1/8 W, 5%
R12	Fusible Resistor
R15	5.1K, 1/8 W, 5%
RJ11	RJ11 Telephone Jack
P1	Power Connector
P2	DB25 Female 25-Pin Connector
Y1	21.600 MHz XTAL (Crystek Part #013901)
T1	600Ω 1:1 Transformer (TTC-218)
Z1	MOV Surge Protector, V250LA4
SPEAKER CIRCUIT	
U17	LM386
SPKR	Speaker
C15	1 μF
C17	0.047 μF
C18	220 μF
R2, R13	8.2K 1/8 W
C16	0.1 μF
R14	10Ω

89C124FX External Modem Parts List (Continued)

Part	Description
LED CIRCUIT	
U10	74HC245
U14, U15	74HC373
LDSPLY1, LDSPLY2	HDSP4830
RN1	10K RPAK

Transmit Output Level(1)		
TX 3,2,1,0	**Typ**	**Units**
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK transmit signal levels, they are typically 1 dB lower. All signals are measured at A01. The tolerance for the transmit levels is ±1 dBm.

89C024FT CHIP SET USERS

By including a small number of jumpers in the design, one board may be used to implement either an 89C024FT V.42/V.42bis modem, or an 89C124FX Data/FAX modem.

There are 2 pin differences between the 89C126FX and the 89C026FT, as defined below in Table 5.

Table 5. Differences between 89C024FT and 89C126FX

89C026FT Pin	89C126FX Pin	Pin Number
$\overline{SI}$	BS0	32
$\overline{TM}$	BS1	39

On the 89C126FX, $\overline{SI}$ and $\overline{TM}$ are memory mapped.

In addition to the pin redefinitions above, there are name differences between the 89C126FX and the 89C026FT, as specified in Table 6. Note that these are changes in name only, not changes in how these pins are used.

Table 6

89C024FT Name	89C124FX Name	Pin Function	Pin Number
CLKIN	X1	Crystal Input	67
TCL0	NVCLK	NVRAM Clock	19
TCL1	NVDATA	NVRAM Data	20
S/A	$\overline{NVCE}$	NVRAM Chip Enable	21
CDE	V_{SS3}	Digital Ground	14

With the 89C124FX chip set, the system crystal must be connected to the 89C126FX microcontroller. The crystal cannot be connected to the 89127 as it can be with the 89027 AFE. For this reason, the X1 crystal input, pin 23 on the 89027 is renamed CLKIN on the 89127 AFE. The X2 and CLKOUT pins of the 89027 are not needed on the 89127, and are redefined as described in Table 7 below.

Table 7. Differences between 89027 and 89127

89027 Pin	89127 Pin	Pin Number
X2	$\overline{UCLKEN}$	25
CLKOUT	UARTCK	26
N/C	CLKSEL	22

The 89127 Analog Front End produces a clock signal, UARTCK, which replaces the UART crystal required for internal modem designs. UARTCK is enabled via the $\overline{UCLKEN}$ pin.

UARTCK Specifications
Average Frequency is 1.851 MHz ±0.01% (%deviation from 1.8432 MHz is an average of 0.466%)

NOTE:
$\overline{UCLKEN}$ must be tied to V_{SS} to enable UARTCK. If $\overline{UCLKEN}$ is pulled up, UARTCK is disabled.

Reference Documents

The following materials are available to help you with your 89C124FX based design. To obtain these materials, please contact your local Intel Sales Office.

- Modem Hardware Reference Manual (Order Number: 296235)
- Modem Software Reference Manual (Order Number: 296503)
- 89C124FX Design Guide (Order Number: 297161)

The DCA/Intel CAS specification is available through Intel by calling 1-800-538-3373.

The EIA/TIA-578 Asynchronous Facsimile DCE Control Standard specification is available through EIA Standards Sales Department at (202) 457-4966.

89C124FX Revision History

The following differences exist between revision -001 and this version of the datasheet:

1. Schematics and Parts List section and Memory Address Logic Section added.
2. Crystal Specification changed.
3. QFP packaging information added.
4. The address of R. Scott Associates on page 1 has changed.
5. S101 and S102 descriptions have been added to the Configuration Registers Section.
6. Reference Documents section updated.

intel®

AB-24

APPLICATION BRIEF

89024 Modem Customization for V.23 Data Transmission

BRIAN D. WALSH
APPLICATIONS ENGINEER
INTEL CORPORATION

May 1989

Order Number: 292058-001

89024 MODEM CUSTOMIZATION FOR V.23 DATA TRANSMISSION

CONTENTS

INTRODUCTION

This application brief will illustrate the steps involved in customizing a modem application using the 89024 modem chip set. Specifically, it will show how one may add V.23 capability to an 89024 modem design as embodied in the MEK II (Intel Modem Evaluation Kit) running software version 3.2.

GENERAL DESCRIPTION

This design consists of using the 89026 processor to control a separate V.23 Data Pump IC (Texas Instruments TCM3105) to support V.23 modulation in addition to the currently supported V.22bis/V.22/V.21/Bell212/Bell103.

The modem is placed in V.23 mode using the "AT&A1" command and is returned to normal operation with the "AT&A0" command. The originating modem dials normally using "AT" commands and then 2 seconds after completion of dialing, the modem sends 75 bps V.23 carrier. The answering modem, upon detecting a ring signal, goes off hook and sends 1200 bps V.23 carrier. The originate modem sends data at 75 bps and receives data at 1200 bps, while the answer modem sends at 1200 bps and receives at 75 bps. Both respond to "escape" at 1200 bps and command mode is always at 1200/1200 bps. The V.23 transmit level is fixed. Backward channel CCITT circuits are not supported, data is always transmitted from pin 2 and received at pin 3.

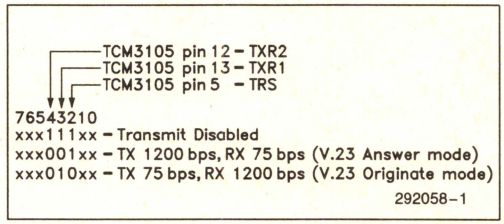
This application brief does not address the issues of V.25 calling tones or V.25 calling station identification.

HARDWARE DESCRIPTION

The MEK II is modified by adding a Texas Instruments TCM3105 FSK Modem IC. This Modem chip does not have an on-chip 4-wire to 2-wire hybrid circuit, so we use a dual op-amp MC1458 for this purpose. In order to control the TCM3105 we use 3 additional outputs of the 74LS373 latch that is already used to latch the /JS and AA signals from the microcontroller address/data bus. A 74LS157 2- to 1-line data selector is used to select the source of received data and the source of "energy detect" signal to the microcontroller.

V.23 Modem IC

The TCM3105 (U102) is a CMOS V.23 modem in a 16-pin package that consumes only 40 mW. It requires an external 4.4336 MHz crystal connected between pins 15 and 16 to derive timing. A resistor divider sets the carrier detect threshold by adjusting the voltage at pin 10. Bias distortion may be minimized by adjusting the voltage at pin 7. Pins 5, 13 and 12 together set the various modes of operation. These pins are connected to pins 6, 9 and 12 respectively of 74LS373 (U18) and are controlled through bits 2, 3 and 4 and executing a "STore" instruction to any even address of external memory (since this is the only external memory to be used). The modes of interest to us are:



74LS157 Data Selector

This IC is always enabled and the select signal is connected to the 6th output (bit 5) of the 74LS373 latch (U18). "SToring" a "0" to bit 5 of the latch selects "normal" mode of operation, while "SToring" a "1" to bit 5 selects V.23 mode. During "normal" mode, Receive Data (RXD) is routed from the 89026 microcontroller to the DTE and Energy Detect (ED) is routed from the 89027 AFE to the microcontroller. During V.23 mode RXD goes from the TCM3105 to the DTE and ED goes from the TCM3105 to the microcontroller. Transmit Data (TXD) is always connected from the DTE to both the 89026 and the TCM3105.

MC1458 Dual Op-Amp

This IC is configured as an active hybrid circuit, converting the 4-wire transmit and receive signals to 2-wire to drive the line transformer. The transmitted signal is also summed, but since only one of the transmitters will be active at a time, this will not be a problem. The 89027 has pin 10 tied low so as to disable the AFE's on-chip hybrid.

A schematic diagram of these changes is shown in Figure 1.

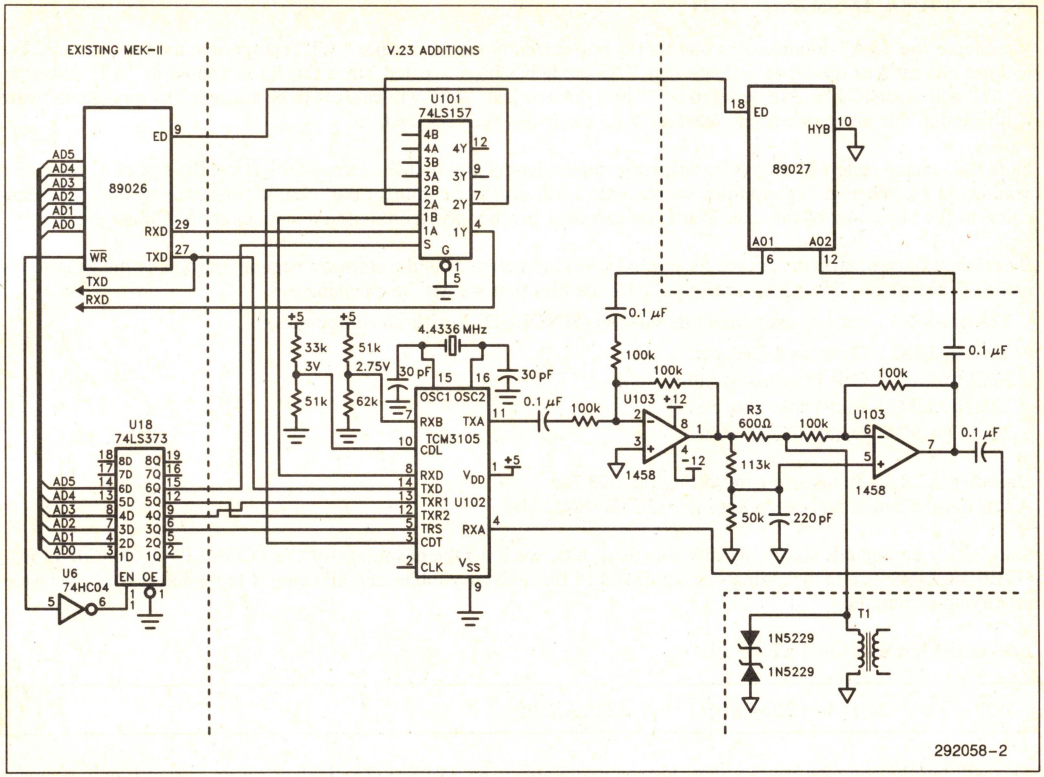


Figure 1. Schematic Diagram

SOFTWARE DESCRIPTION

We choose the "&A" command as one that is not currently used by major "AT" compatible modem vendors. We will use S23 bit 3 as the bit to indicate that V.23 mode has been selected, since this bit is unused in "AT" modems. "&A1" will cause S23 bit 3 to be set to a "1" and &A0 or just "&A" will cause it to be cleared. The modem software will examine this bit to determine whether V.23 mode has been selected.

Note that source code will always be written in capital letters and that the assembler ignores the rest of a line after a semi-colon (;). When giving modified source code I will usually "comment out" the original code by adding a semi-colon to the beginning of the line. This is an excellent practice to facilitate the documentation of changes.

By convention we name the source files: nmxxx.SRC (where n.m is the software version and xxx is the generic file name). Since we are using software version 3.2 the files that we will be changing are:

32AAD.SRC register assignment definitions ($INCLUDEd with all source files)
32CMD.SRC Command Decoder
32CPM.SRC Call Progress Monitor routines
32HND.SRC Handshake routines
32DATA.SRC Data Mode routines

Decoding AT&A1 Command and Setting the S23 Bit
All of these changes will be done to the 32CMD.SRC file.

Since many commands simply modify S-register bits, we can take advantage of the "COMMON_REGISTER_OPERATIONS:" code by adding our command to the necessary tables and allowing it to be decoded as a register-modifying command.

Add as the last entry in TABLE_1:

```
DCB   (3 * 32) + (S23-S0)      ; AND_A_CMD
```

This will tell the common routine that this command affects bit 3 of S23. The table is set up so that it only occupies one byte per entry, with the bit number in the upper 3 bits and the register number in the lower 5 bits.

Add the command to the command list and the command vector table:

```
AND_CMDS:      DCB   "CJLPRSDG'
;              DCB   "MXFWZT',     0   ; was like this
               DCB   "MXAFWZT',    0   ; added &A command betw X and F
```

```
CMD_LU_TBL:    ....
               ....
;    DCB   AND_G_CMD-G1, AND_M_CMD-G1, AND_X_CMD-G1, AND_F_CMD-G2
     DCB   AND_G_CMD-G1, AND_M_CMD-G1, AND_X_CMD-G1, AND_A_CMD-G1
     DCB   AND_F_CMD-G2
```

The command vector table is the address offset of the command label from that of the first command (G1 EQU A_CMD). In the interests of saving space this offset table is only 1 byte per entry and so it has to be split into 2 groups as the range of addresses of command labels is more than 255 bytes. When modifying command code it is worth checking the list file to make sure that the CMD_LU_TBL: entries do not get bigger than 0FFH and wrap around through 0, causing those commands to branch to the wrong address.

Fix the branch vector calculator and the dial command offset calculator because the 1st group of commands are now 33 instead of 32:

```
GENERATE_BRANCH_VECTOR:
     ADD  TEMP_CMD_3, #G1              ; ADD OFFSET TO 1ST CMD GROUP
;    CMPB TEMP_CMD_2, #32              ; FIRST 32 CMDS FIT IN
     CMPB TEMP_CMD_2, #33              ; FIRST 33 CMDS FIT IN
```

```
D_R_CMD:
;    SUBB  CPM_CONTROL, TEMP_CMD_2, #36
     SUBB  CPM_CONTROL, TEMP_CMD_2, #37
```

Add the command label with the rest of the register modifying commands:

```
Y_CMD:
AND_A_CMD:    ; added &A command for V.23 operation
AND_C_CMD:
```

Updating the Output Pins to Control the TCM3105 and Data Selector

The IO_CONTROL: section of code in file 32CMD.SRC runs all the time and could be considered the "background routine". This is where the RS232 leads are updated, the health of the other routines is checked and the 74LS373 latch (U18) is written and is thus an appropriate place for the TCM3105 chip and the Data Selector (Data Mux) to be updated.

Add the following code after END_JS_UPDATE:

```
END_JS_UPDATE:

V_23_UPDATE:
  ANDB TEMP_CMD_1, #11011111B       ; MUX TO NON-V.23 POSN
  ORB  TEMP_CMD_1, #00011100B       ; SET V.23 CHIP OFF
  JBC  S23,  3, END_V_23_UPDATE     ; JMP IF NOT IN V.23 MODE

  JBC  CNTRL_C, 1, END_V_23_UPDATE ; JMP IF NOT IN HND OR DATA MODE
  ANDB TEMP_CMD_1, #11100111B       ; SET V.23 CHIP TO ANS MODE
  ORB  TEMP_CMD_1, #00000100B

  JBC  S14, 7, NOT_ORIG_MODE        ; JMP IF S REG SET TO ANS MODE
  ANDB TEMP_CMD_1, #11101011B       ; SET V.23 CHIP TO ORIG MODE
  ORB  TEMP_CMD_1, #00001000B

NOT_ORIG_MODE:
  JBC  CNTRL_C, 0, END_V_23_UPDATE ; JMP IF NOT IN DATA MODE
  JBS  CNTRL_C, 2, END_V_23_UPDATE ; JMP IF CMD FUNCTS ENABLED
  ORB  TEMP_CMD_1, #00100000B       ; DATA MODE, SO MUX TO V.23 POSN

END_V_23_UPDATE:
```

The next instruction in the source code STores the contents of TEMP_CMD_1 to PORT3, and so updates the Data Mux.

In order to ensure that the Data Mux gets set before the "OK" message is sent when entering the on-line escape state (response to "+ + +"), add a line of code after the three "ORB" instructions:

```
VALID_ESCAPE_SEQUENCE:
  ORB  CNTRL_F, #00010000B          ; ENABLE ESCAPE STATE
  ORB  CNTRL_C, #00000100B          ; ENABLE CMD FUNCTIONS
  ORB  MSG_RQST, #00100000B         ; SEND "OK" MESSAGE WITH MSG RQST
  JBS  S23, 3, ESCAPE_DETECT_END ; TRICK TO FORCE 1 MORE PASS THRU
       ; IO_CONTROL FOR MUX SETUP BEFORE GOING TO COMMAND DECODER
```

After a dial command is executed by the Command routine, it will activate the Call Progress routines.

The V.23 Call Progress Monitor Routines

The 32CPM.SRC routines check for call progress signals on the phone line and also for answer tone from the remote answering modem. Since a V.23 modem will answer with a 1300 Hz tone (1200 bps mark frequency), the AFE receive filter must be set to V.22 answer mode so as to pass this frequency to the energy detect circuitry.

Add three lines of code at the label SET_ANSWER_CONT:

```
SET_ANSWER_CONT:
  ANDB CPM_FLAG, #11101111B ; FLAG ANSWER PROCESSING FOR HOUSEKEEPING

  JBC  S23,  3, SET_ANSWER_CONT_1 ; IF V23 MODE THEN
  LDB  AFE_BYTE3, #01000000B      ; SET FILTER TO QAM ANS FOR
SET_ANSWER_CONT_1:                ; 1300Hz CARRIER DETECTION

  SJMP SIGNAL_MONITOR_INIT
```

The CPM routines will hand over control to the Handshake routines which we need to modify for V.23 handshake.

The V.23 Handshake Routines

The Handshake mode 32HND.SRC is entered for the first time after successful completion of the Call Progress routines. The first time that HANDSHAKE_MODE: is called, it goes through the Initialization code before the main routine is executed, thereafter the Initialization is skipped. The Main routine is entered at a rate of 600 times per second or more and consists of checking for Energy Detect and then branching to the routine address saved in TX_RTN_ADDR. The logical flow of the handshaking is controlled by changing the contents of TX_RTN_ADDR to the address of the routine to be executed the next time Handshake is called.

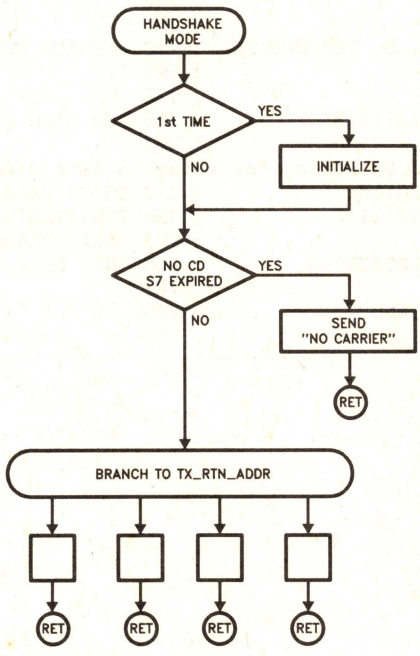


Figure 2

The Initialization required for V.23 consists of starting the S7 wait-for-carrier timer, starting a 2 second timer and loading a return address for the next time the routine executes. The following lines of source code are added (identified by "V23" at the start of the comment field) to the Handshake Initialization:

```
HANDSHAKE_INIT:
  ANDB MODE_STATUS, #10111111B          ; CLEAR INIT FLAG
                                        ; V23
  JBC  S23,  3,  NOT_V23_INIT           ; V23
V23_HND_INIT:                           ; V23
  ADDB S7_TIMER, TIME_BASE_SECOND, S7   ; V23 INIT S7 DCD TIMER
  ADDB TX_TIMER, TIME_BASE_100MS, #20D  ; V23 INIT 2 SEC TIMER
  LD   TX_RTN_ADDR,   #V23_HND_WAIT     ; V23
  SJMP HND_INIT_END                     ; V23
                                        ; V23
NOT_V23_INIT:                           ; V23
```

After the initialization code is executed once, the software will keep branching to V23__HND__WAIT: until the 2-second timer has expired, then it will initiate a "CONNECT" message. While the Connect message is being sent, the software will branch to V23__HND__MESSAGE:, then it will set up the Data mode and thereafter the Data Mode will be called instead of the Handshake mode.

```
V23_HND_WAIT:                           ; V23
  CMPB TIME_BASE_100MS, TX_TIMER        ; V23 TIMER EXPIRED YET?
  JNE  V23_HND_END                      ; V23
V23_HND_MESSAGE_INIT:                   ; V23
  LDB  MESSAGE_REQUEST, #00100001B      ; V23 START CONNECT MESSAGE
  LD   TX_RTN_ADDR,   #V23_HND_MESSAGE  ; V23
  SJMP V23_HND_END                      ; V23
                                        ; V23
V23_HND_MESSAGE:                        ; V23
  JBS  MESSAGE_REQUEST, 5, V23_HND_END  ; V23 MESSAGE SENT YET?
V23_HND_MESSAGE_END:                    ; V23
                                        ; V23
  ANDB COPY_PORT4, #10111111B           ; V23 DCD HIGH AFTER CONNECT
V23_SET_UP_DATA_MODE:                   ; V23
; This is where we need to set up for going to data mode
  ORB   CNTRL_C, #00000011B             ; V23 GO TO DATA MODE
  ANDB  AFE_BYTE4, #00111111B           ; V23 TXMITTER OFF, AFE OFF
  CLRB  DM_FLAGS                        ; V23 CLEAR FLAGS FOR DM
  ORB   MODE_STATUS, #10000000B         ; V23 INIT DATA MODE
V23_HND_END:                            ; V23
  LJMP  HANDSHAKE_MODE_END              ; V23
                                        ; V23
```

V.23 Data Mode

The modifications required in the Data Mode consist of checking for V23 mode and skipping past:

Initialization
Send space disconnect (twice)
Receive space disconnect
Loss of carrier disconnect
Retrain request
Test mode

```
DATA_MODE_INIT:
; DM FLAGS ALREADY CLEARED IN HANDSHAKE MODE
  ANDB MODE_STATUS,#7FH                ; CLEAR INITIALIZE FLAG
  JBS S23, 3, DATA_MODE_INIT_END       ; IF V23 THEN INIT DONE
```

```
DISCONNECT_INIT:
  ANDB DM_FLAGS, #11111101B            ; CLEAR DISCONNECT INIT FLAG
  JBS  S23,  3,  HANG_UP               ; V23 FORGET SPACE DISCONNECT
```

```
SEND_SPACE:
  JBC  S21, 7, HANG_UP                 ; IF BREAK_DISCONNECT DISABLED
  JBS  S23, 3,  HANG_UP                ; V23 FORGET BREAK
```

```
CHECK_DISCONNECT:                      ; CHECK FOR LONG SPACE DISC
CHECK_BREAK:
  JBS  S23, 3,  SET_BREAK_TIME         ; V23 FORGET BREAK
```

```
CHECK_CARRIER_LOSS:
  JBS  PORT0, 7, CHECK_CARRIER_LOSS_END ; SKIP IF ED IS HIGH
  ORB  DM_FLAGS, #01000000B             ; SET CDLOSS FLAG
  ADDB EDOFF_TIME,TIME_BASE_100MS,S10 ; CDOFF THRESHOLD IN REGISTER
  INCB EDOFF_TIME                 ; PUT AN OFFSET IN TIME FOR PROPER
                                        ; OPERATION DURING TM EXIT
  JBS S23, 3, CARRIER_LOSS_END          ; ALL DONE IF V23 MODE
```

```
QAM_RETRAIN:
  JBS S23, 3, SJMP_CHECK_TEST_MODE    ; SKIP RETRAIN IF V23 MODE
```

```
CHECK_S16_STATUS:
; EXAMINE S16 REGISTER FOR ANY TEST MODES AND SET FLAG
  JBS S23, 3, CHECK_S16_STATUS_END    ; SKIP RETRAIN IF V23 MODE
```

Assembling the Source Files
The source files can be assembled by issuing the following commands at the DOS prompt:

```
ASM96 32CMD.SRC
ASM96 32CPM.SRC
ASM96 32HND.SRC
ASM96 32DATA.SRC
```

Linking the Object Files
Link the object files by issuing the following command at the DOS prompt:

```
RL96 32HND.OBJ, 32INIT.OBJ, 32CMD.OBJ, 32CPM.OBJ, 32DATA.OBJ,
     32SOFT.OBJ, 32HSI.OBJ, 32HSO.OBJ, 32RX.OBJ TO 32ATR
```

Programming the EPROMs
After the code has been linked and located, the code must be split into low and high byte segments for programming into EPROMS. The following IPPS session illustrates that process (IPPS prompts are not shown):

```
IPPS                          ; invoke IPPS
I 80                          ; initialize file format
FORMAT 32ATR                  ; filename resulting from linking
3                             ; logical unit is byte
2                             ; input file is in words (2 bytes)
1                             ; output file is in bytes
0 to  32ATR.LO                ; low order bytes to one file
1 to  32ATR.HI                ; high order bytes to another
<enter>                       ; press "enter" to exit formatting
                              ;
                              ; the following assumes that an
                              ; INTEL PiUP 201A programmer is
                              ; connected to the PC
                              ;
TYPE                          ; display available EPROM types
27128                         ; specify EPROM type
                              ; insert blank EPROM into programmer
COPY 32ATR.LO TO PROM         ; copy low byte file to prom
                              ; insert blank EPROM into programmer
COPY 32ATR.HI TO PROM         ; copy low byte file to prom
EX                            ; exit IPPS
```

Custom routines can now be tested by placing EPROMS into target hardware.

REFERENCES

1. "FSK Modems: TCM3105 Designers Information" from Telecommunications Circuits Data Book, 1986. By Texas Instruments.
2. MEKII 89024 Enhanced Modem Evaluation Kit Users Manual, 1987. By Intel Corp.
3. 89024 Modem Reference Manual, 1987. By Intel Corp.
4. Developing MCS-96 Applications Using the SBE-96. Application Note AP-273 (Order Number 280249-001). By Intel Corp.

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AP-366

APPLICATION NOTE

1

89C124FX Data/FAX Modem Chip Set

Reduction of Power Consumption

JIN LIEN LIN
TECHNICAL MARKETING ENGINEER

November 1992

Order Number: 292101-001

89C124FX Data/FAX Modem Chip Set
Reduction of Power Consumption

CONTENTS

INTRODUCTION

The 89C124FX Data/Fax Modem Chip Set Application Note provides the end user with applications and layout guidelines to reduce power consumption to a minimum when in the Power Down Mode.

GENERAL DESCRIPTION

When the 89C124FX is in the power down mode, the microcontroller (89C126FX) consumes very little power (less than 0.5 mW). However, the external memory, voltage regulators and peripherals draw excess current that makes the overall system power consumption more than 80 mW. This application note describes a method to reduce overall system power consumption to less than 1 mW when the 89C124FX is in the power down mode. Adding a power down feature in the microcontroller and reducing power sink to a minimum accomplishes this goal.

Three steps are required to reduce the overall system power consumption in the power down mode:

1. Detect power down in the microcontroller and isolate the power source from potential current sink from other components.
2. Inhibit the DC path from the power supply, through other components, to ground when the microcontroller is powered down.
3. Solve current drift problems due to floating inputs when power is removed from peripherals.

POWER DOWN DETECTION

Monitoring the clock output (CLKOUT, pin 65) from the microcontroller detects the power down condition. The CLKOUT pin is held high when the controller is in the power down mode. When power down is detected, the detector shuts off the +5V supply to all components except the microcontroller, RAM, and logic gates. The detector also shuts off power to the voltage regulators.

BLOCKING DC PATH

When the power down detector shuts off the bipolar switches, some of the device input pins become current sinks and drain current from the controller output pins when the output pins are high. These controller output pins are the CLKOUT and SCLK outputs. To eliminate these DC paths in the power down mode, add an inverter from the controller clock output (CLKOUT) to the AFE clock input (CLKIN) and use an AND gate to change the SCLK output to the AFE to a low.

CURRENT DRIFT

When the controller is in the power down mode, the SDATA pin becomes a floating input that can draw current in excess of 300 μA. Placing a 510 KΩ resistor between SDATA pin and ground solves this problem. Using a 100 KΩ resistor or lower may impede circuit functionality.

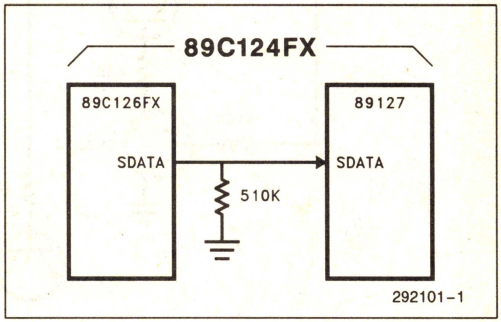

Figure 1. Placement of Current Drain Blocking Resistor

DESIGN TRADE OFF

The reduced power drain feature design trade-off, besides adding circuit complexity, is an additional 20 mW power consumption when the 89C124FX is active.

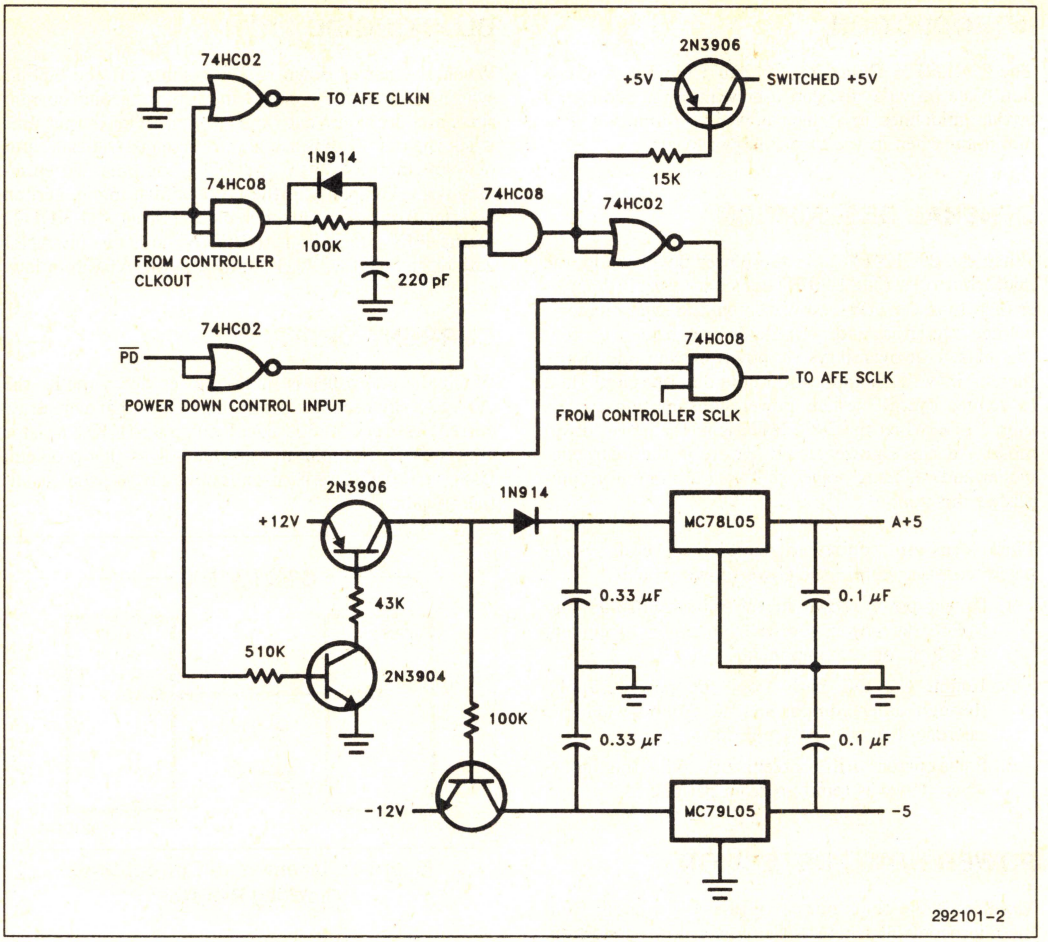

Figure 2. 89C124FX Power Consumption Circuit Modifications

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APPLICATION NOTE

1

89C124FX Data/Fax Modem Chip Set

Printed Circuit Layout Guidelines

JACK ST. CLAIR
DAVE OBERBECK
TECHNICAL MARKETING

October 1992

Order Number: 292104-001

89C124FX Data/Fax Modem Chip Set

CONTENTS

CONTENTS

1.0 INTRODUCTION

This 89C124FX Data/Fax Modem Chip Set Application Note provides layout guidelines to build the chip set onto printed circuit boards with maximum design definition. These guidelines help prevent noise injection into sensitive analog circuits and help insure the highest performance characteristics, lowest bit error rate and highest throughput. This is especially true when the board is used in the Fax mode.

2.0 THE 89C124FX DATA/FAX MODEM CHIP SET

The Intel 89C124FX is a highly integrated, Send and Receive data-fax modem chip set. This two chip solution is composed of the 89C126FX microcontroller and the 89127 Analog Front End (AFE). The 89C124FX features 9600 bps Send and Receive FAX, V.42/V.42bis error correction and data compression, low power consumption, easy upgrade from other Intel modem chip sets, and ease of use via the Intel/DCA Communicating Applications Specification (CAS).

The 89C126FX microcontroller executes DSP algorithms for modulation, demodulation, and data formatting. It also performs the AT and EIA/TIA-578 command set interface functions, and error correction and data compression. The 89C126FX comes in a 68-lead PLCC package.

The 89127 AFE provides D/A conversion, filtering, AGC, 2 wire hybrid conversion and telephone line data access arrangement (DAA) interface. The 89127 comes in 28-lead PLCC and 28-lead PDIP packages.

Reference designators called out in the text are from the schematics included with this document.

3.0 89127 ANALOG FRONT END

Suggested placement of the following components is designed to achieve optimum performance characteristics of the 89C124FX Chip Set.

AFE Placement: Place the AFE on the circuit board as close as possible to the modem controller. Place the DAA circuits very close to the AFE as well, in a direction opposite that of the modem controller.

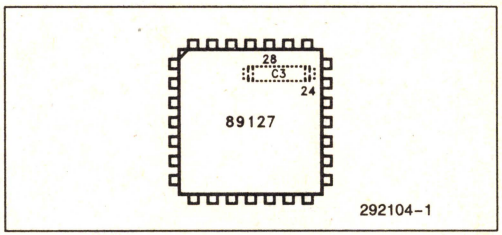
Autozero Capacitor, C3: Locate the autozero capacitor, C3, on the same side of the circuit board as the AFE and as close as is physically possible. Ensure that there are no traces running between the capacitor and the AFE as this is a very sensitive part of the circuit. Any noise coupling into these nodes directly affect bit error rate performance.

NOTE:
The Analog −5V Decoupling supply input circuit is extremely sensitive to noise. Ensure care is taken when implementing changes to this circuit.

Analog −5V Decoupling: Physically locate the Analog −5V Decoupling regulator very close to the AFE, away from the DAA. The Decoupling capacitor on the output (C18) must be very close to regulator (U10). Place another capacitor (C4) right next to the AFE.

To maximize circuit performance, allowance can be made for a filter bead (similar to L1) to be placed in series with the output of the regulator to overcome any spurious noise occurrences.

Analog +5V Decoupling: As with the −5V supply, the regulator that supplies this voltage should be physically very close to the AFE, away from the DAA. The decoupling capacitor on the output (C17) should be very close to the regulator (U9). Place a 100 nF ceramic decoupling capacitor across leads 28 and 24 of the AFE as close as possible to the chip. All circuit traces from this capacitor to the ground and power planes must be a minimum of 0.050 inches thick. It may be necessary to place the capacitor on the back side of the board as shown.



Hybrid Resistors: Place resistors R6 and R7 immediately beside the AFE at pin 6. No circuit traces should run between these resistors and the AFE.

CAUTION:
Noise injected between resistors R6 and R7 and the AFE will appear directly on the receiver circuits. Care should be taken to ensure that these resistors are placed as close to the AFE as possible.

Analog Ground/Digital Ground: These two ground signals should be connected together at one point only at the AFE with a trace that runs from the AGND (pin 12) of the controller to the V_{SS} (pin 24) of the AFE to the ground plane of the board. This circuit trace must be a minimum of 0.050 inches thick.

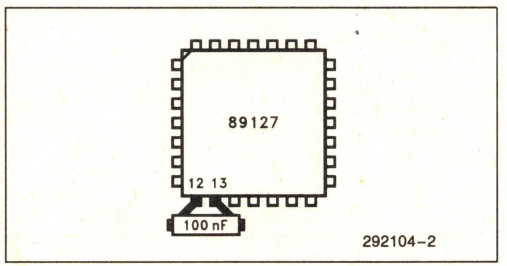
4.0 89C126FX MODEM CONTROLLER

As with the AFE, placement of the following components is designed to achieve optimum performance characteristics of the 89C124FX Chip Set.

Crystal and Capacitors: Crystal Y1 and capacitors C1 and C2 should be physically very close to the modem controller chip. No traces should run underneath the leads between the crystal and the controller, and there should be no leads running between the capacitors and the crystal. This ensures stability and absolute accuracy of the crystal.

Decoupling Capacitor: Place a 100 nF ceramic decoupling capacitor across pins 68, 36 and 1 of the controller as close as possible. All traces from this capacitor to ground and power planes must be a minimum of 0.050 inches thick.

Analog +5V Decoupling: Place a 100 nF ceramic decoupling capacitor (not shown on schematic) right next to the controller between analog ground (pin 12) and V_{REF} (pin 13) of the controller as shown.



V_{PP} Suppression Capacitors: The V_{PP} suppression capacitors C5 and C6 should be placed on the circuit board very close to the controller.

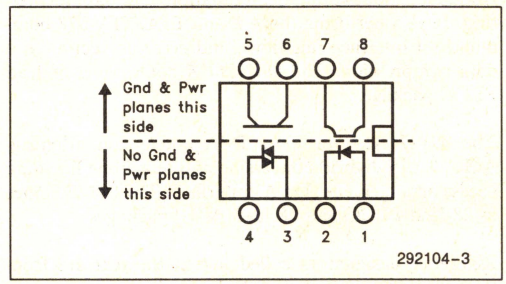
5.0 GENERAL POWER CONSIDERATIONS

Incoming Power Filtering: The aluminum electrolytic cap C23 should be located immediately next to the incoming power pins. Another 100 nF ceramic cap should be next to it to help filter out the higher frequencies that are present on incoming power. You may want to consider a filter bead (like L1) on the incoming 5V as well.

Memory Power Decoupling: Place 100 nF ceramic capacitors right next to U4, U5, and U6. Add an additional two capacitors between U3, U7, U12 and U13 (any combination will suffice).

6.0 DAA CIRCUITRY

In general, follow the requirements for FCC Part 68. Refer to Intel Modem Hardware Reference Manual. In addition, the following layout guidelines must be followed. Do not place ground or power planes beneath the "hot" side of the DAA as shown in the attached figure. Component shown is an Analog Opto-Isolator, Theta-J, Model TS120.



Ensure that the traces between the RJ11 phone jack and MOV (Z1) are a minimum of 0.04 inches.

Ensure that the traces between MOV (Z1) and T1 and the opto-isolator are a minimum of 0.02 inches.

Maintain a minimum gap of 3mm between traces on the "hot" side of the DAA and the remainder of the circuitry.

7.0 REFERENCE DOCUMENTS

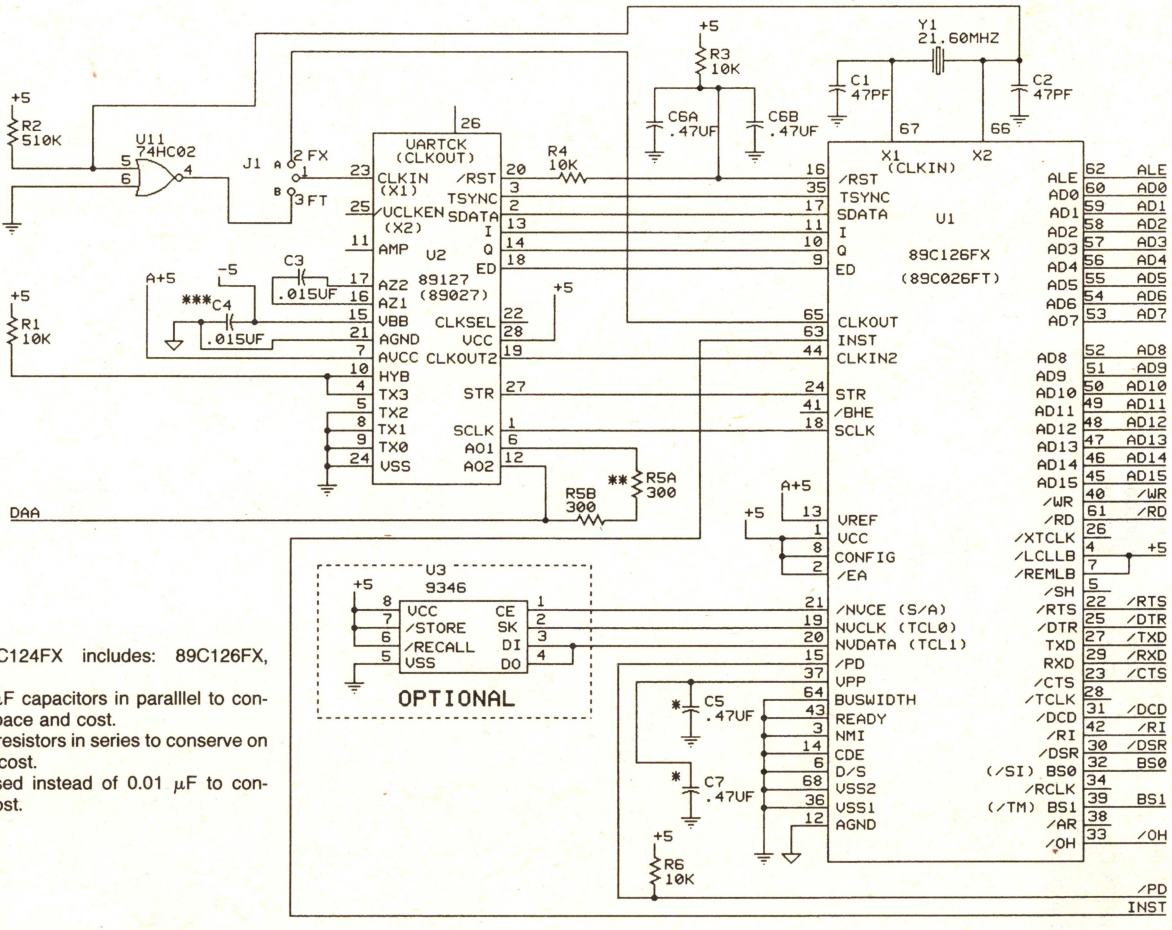
The following document provides additional layout guidelines for the reduction of power consumption when in the power down mode.

Title	Application Note	Order Number
89C124FX Data/Fax Chip Set Reduction of Power Consumption	AP-366	292101

8.0 SCHEMATICS

The attached schematic diagram represents a typical application layout. For additional information, contact your local Intel representative.

Chip Set



292104-4

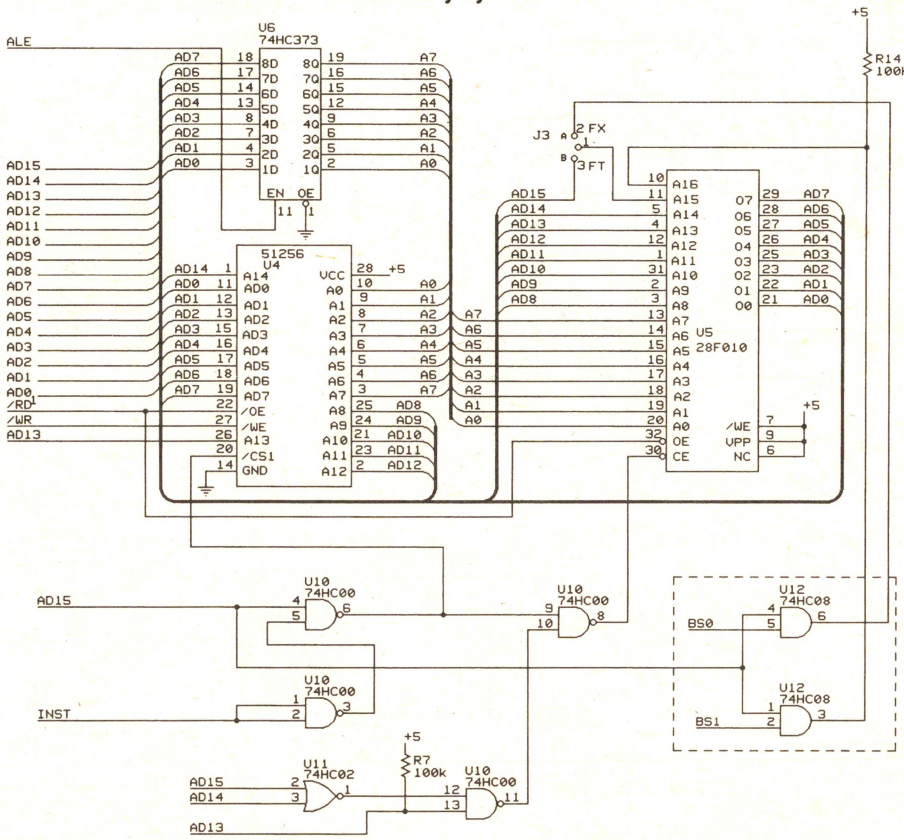
NOTES:
Chip Set 89C124FX includes: 89C126FX, 89127.

*Two 0.47 μF capacitors in paralllel to conserve on space and cost.

**Two 300Ω resistors in series to conserve on space and cost.

***0.15 μF used instead of 0.01 μF to conserve on cost.

Memory System



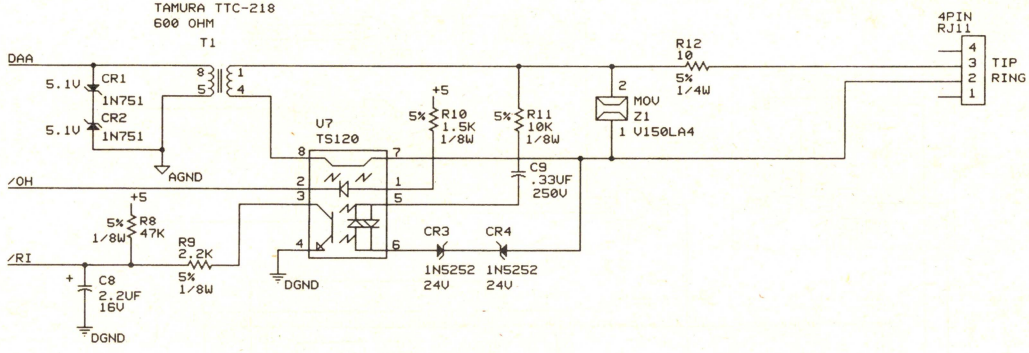
Do not populate R14 for FX.

Do not populate U12 for FT.

292104-5

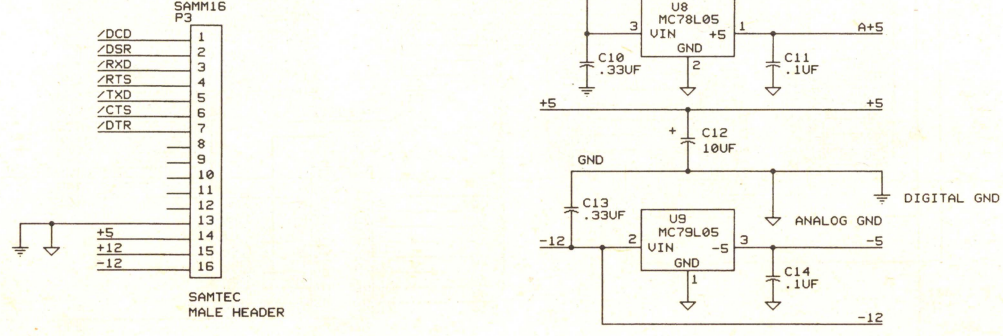
NOTES:
Tie all space inputs to GND.
All IC's to be bypassed with 0.1 μF caps, V_{CC} to GND.
Jumpers must be connected for operation of specific version.

DAA



292104-6

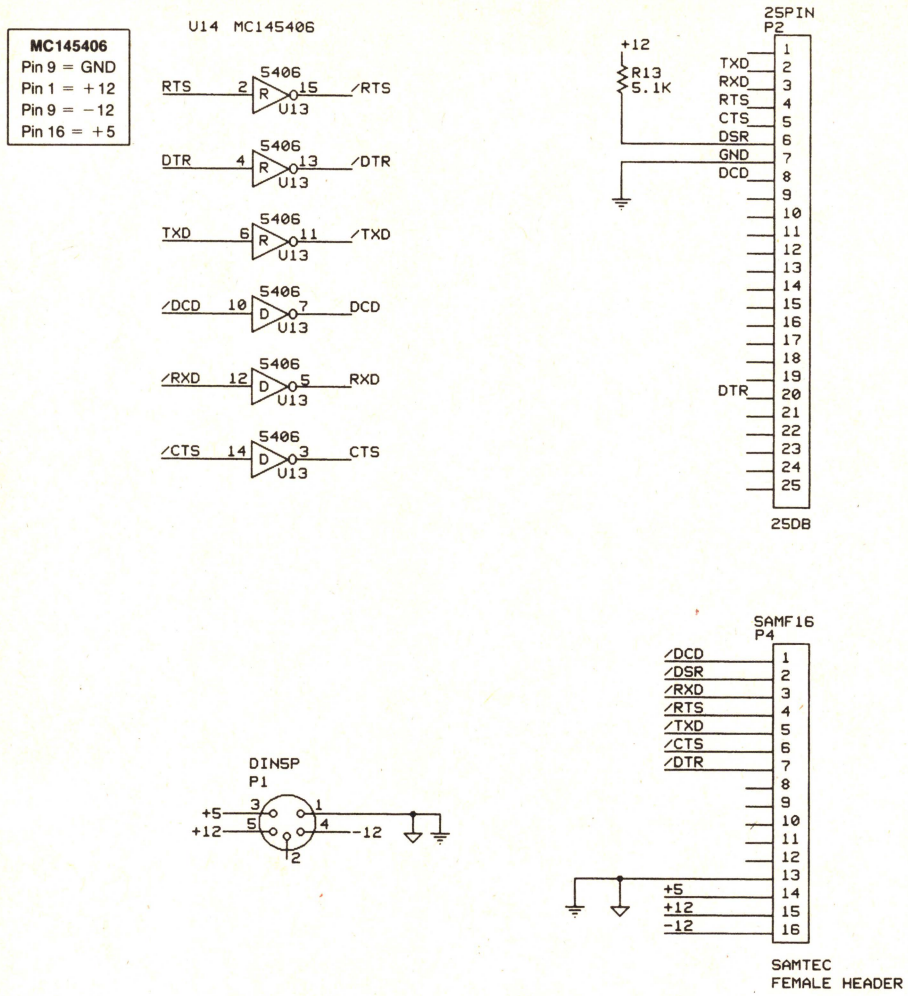
Power



292104-7

NOTE:
Mfgr pinouts for regulators vary, this schematic incorporates Motorola parts.

RS-232 Adapter



Telecommunication Products 2

2910A
PCM CODEC - μLAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G712 Compatible, ATT T1 Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Timeslot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots are Used**
- **±5% Power Supplies: +12V, +5V, −5V**
- **78dB Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel 2910A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

The primary applications are in telephone systems:

- Transmission —T1 Carrier
- Switching —Digital PBX's and Central Office Switching Systems
- Concentration —Subscriber Carrier/Concentrators

The wide dynamic range of the 2910A (78dB) and the minimal conversion time (80μsec minimum) make it an ideal product for other applications, like:

- Date Acquisition • Telemetry • Secure Communications Systems • Signal Processing Systems

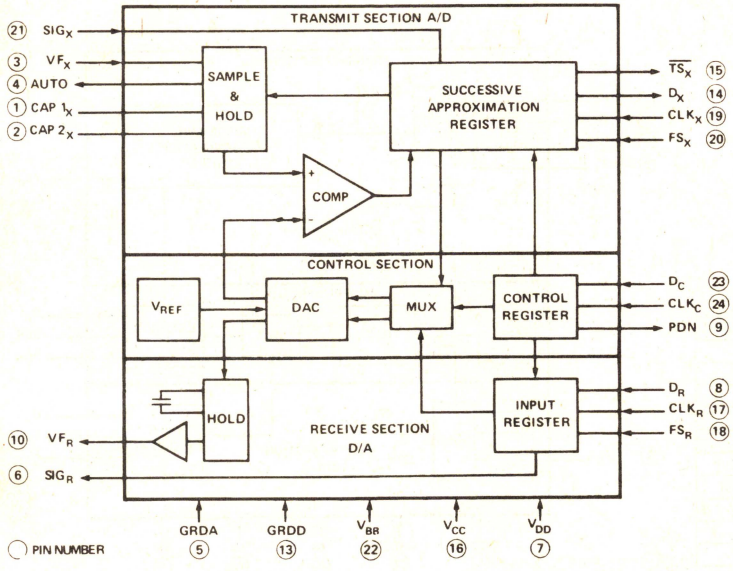


Figure 1. Block Diagram

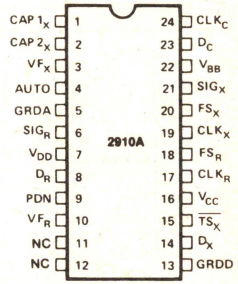


Figure 2. Pin Configuration

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C, SIG_X	Digital Input
SIG_R, D_X, $\overline{TS}_X$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

Figure 3. Pin Names

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

November 1986
Order Number: 006785-002

2911A-1
PCM CODEC—A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible, Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots Are Used**
- **±5% Power Supplies: +12V, +5V, −5V**
- **66 dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33 mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

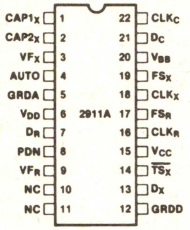
The Intel 2911A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2911A (66 dB) and the minimal conversion time (80 μs minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

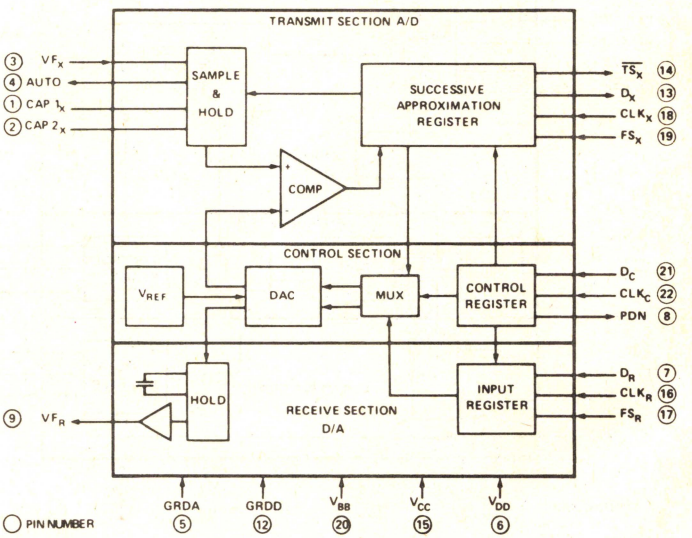


270158-1

Figure 1. Pin Configuration

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C	Digital Input
D_X, $\overline{TS_X}$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

Figure 2. Pin Names



270158-2

Figure 3. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

November 1986
Order Number: 270158-001

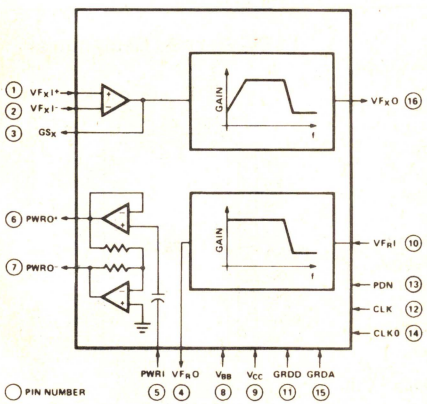
2912A
PCM TRANSMIT/RECEIVE FILTER

- **Low Power Consumption:**
  60 mW Typical without Power Amplifiers
  80 mW Typical with Power Amplifiers
  0.5 mW Typical Standby
- **Low Idle Channel Noise:**
  2 dBrnc0 Typical, Receive
  6 dBrnc0 Typical, Transmit
- **Excellent Power Supply Rejection:**
  40 dB Typical on V_{CC} @ 50 KHz
  30 dB Typical on V_{BB} @ 50 KHz
- **Transmit Filter Rejects Low Frequency Noise:**
  23 dB @ 60 Hz
  25 dB @ 50 Hz
  50 dB @ 16-2/3 Hz
- **Adjustable Gain in Both Directions**
- **Fully Compatible with the Industry Standard Intel 2912**
- **D3/D4 and CCITT G712 Compatible**
- **Common Mode Op Amp Input Rejection 75 dB Typical**
- **Direct Interface to the Intel 2910A/2911A PCM Codecs Including Stand-By Power Down Mode**
- **Direct Interface with Transformer or Electronic Hybrids**
- **Fabricated with Reliable N-Channel MOS Process**

2

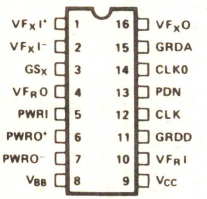
The Intel 2912A 2nd generation PCM line filter is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. It has improved key parameters of power consumption, idle channel noise, and power supply rejection. A single part exceeds both AT&T* D3/D4 and CCITT transmission specs, exceeds digital Class 5 central office switching system stringent specifications, and is fully compatible with the 2912. The primary application for the 2912A is in telephone systems for transmission, switching, or remote concentration.

An advanced version of the switched capacitor technique used for the 2912 is used to implement the transmit and receive passband filter sections of the 2912A. The device is fabricated using Intel's reliable two layer polysilicon gate NMOS technology. (See Intel Reliability Report RR-24 on the 2910A, 2911A, and 2912.) The combination of advances in the switched capacitor techniques first used on the 2912 and the NMOS technology results in a monolithic 2912A filter which is packaged in a standard 16-pin DIP.



270159-1

Figure 1. Block Diagram



270159-2

Pin Names

VF_XI^+, VF_XI^-	Analog Inputs
GS_X	Gain Control
VF_XO	Analog Output
VF_RI	Analog Input
VF_RO	Analog Output
PWRI	Driver Input
$PWRO^+$, $PWRO^-$	Driver Output
CLK	Clock Input
CLK0	Clock Selection
PDN	Power Down
V_{CC}	Power (+5V)
V_{BB}	Power (−5V)
GRDD	Digital Ground
GRDA	Analog Ground

Figure 2. Pin Configuration

*AT&T is a registered trademark of American Telephone and Telegraph Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1988
Order Number: 270159-002

2913 AND 2914
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **2913 Synchronous Clocks Only, 300 Mil Package**
- **2914 Asynchronous Clocks, 8th Bit Signaling, Loop Back Test Capability**
- **AT&T D3/D4 and CCITT Compatible for Synchronous Operation**
- **Pin Selectable μ-Law or A-Law Operation**
- **Two Timing Modes:**
  - **— Fixed Data Rate Mode 1.536, 1.544, or 2.048 MHz**
  - **— Variable Data Rate Mode 64 KHz 2.048 MHz**
- **Exceptional Analog Performance**
- **28-Pin Plastic Leaded Chip Carrier (PLCC) for Higher Integration**
- **Low Power HMOS-E Technology:**
  - **— 5 mW Typical Power Down**
  - **— 140 mW Typical Operating**
- **Fully Differential Architecture Enhances Noise Immunity**
- **On-Chip Auto Zero, Sample and Hold, and Precision Voltage References**
- **Direct Interface with Transformer or Electronic Hybrids**

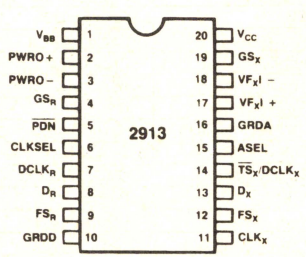
The Intel 2913 and 2914 are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology (HMOS-E). These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2913 and 2914 is superior to that of the separate devices.

The primary applications for the 2913 and 2914 are in telephone systems:

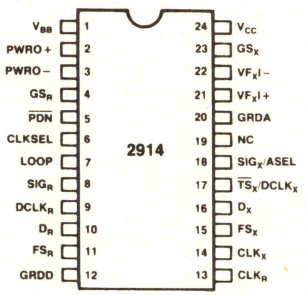
- Switching—Digital PBX's and Central Office Switching Systems
- Transmission—D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments—Digital Handsets and Office Workstations

The wide dynamic range of the 2913 and 2914 (78 dB) and the minimal conversion time make them ideal products for other applications such as:

- Voice Store and Forward
- Digital Echo Cancellers
- Secure Communications Systems
- Satellite Earth Stations

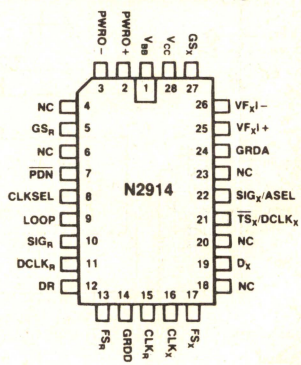


210629-1



210629-2

PLCC 28-Lead Rectangular



210629-3

Figure 1. Pin Configurations

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 210629-004

iATC 29C48
FEATURE CONTROL COMBO

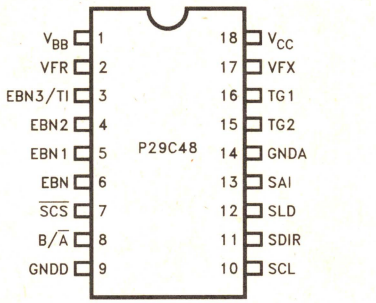
- **External and User Programmable Transmit and Receive Gain**
- **Programmable External Hybrid Balance Network Select**
- **Programmable Analog, Digital and Subscriber Loopback**
- **Programmable μ/A-Law Select**
- **Secondary Analog Input Channel**
- **Low Power Consumption**
- **External Tone Injection to Receive Path**
- **SLD A/B Channel Select (for 16 Channel Line Cards)**

The Intel iATC 29C48 Feature Control Combo is a low cost, user-programmable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C48 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C48 supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog input channel, programmable transmit and receive gain, custom hybrid balancing network selection, and programmable μ or A-law conversions. Additionally, the 29C48 can operate on either the A or B channel of the SLD interface, allowing two combos to be connected to one SLD link. In order to facilitate the SLIC interface in this configuration, the 29C48 generates SLIC chip select signals for the proper routing of signaling information.

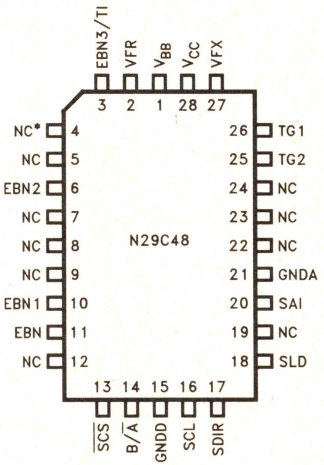
A unique feature of the 29C48 is programmable tone injection. This feature and its SLD interface makes it particularly easy to use in conjunction with Intel's advanced transceivers, such as the iATC 29C53AA, in subscriber equipment environments. The 29C53AA handles transfer of voice and feature control information to the 29C48.

18-Lead Plastic Dual-In-Line Package



270153-1

28-Lead Rectangular Plastic Leaded Chip Carrier



*Not connected

270153-2

Figure 1. Pin Configurations

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 270153-008

Communication/Interface Controllers

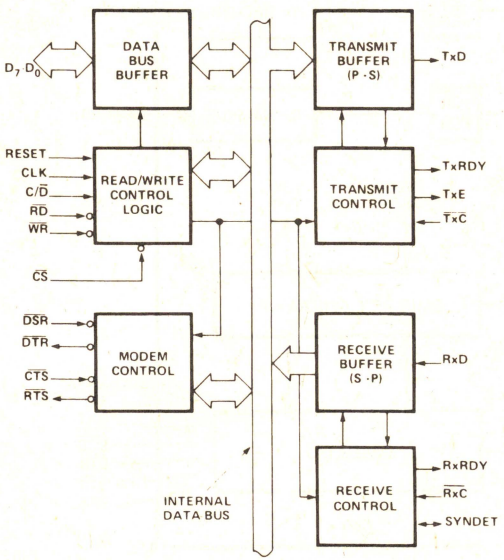
3

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5–8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Synchronous Baud Rate—DC to 64K Baud**
- **Asynchronous Baud Rate—DC to 19.2K Baud**
- **Full-Duplex, Double-Buffered Transmitter and Receiver**
- **Error Detection—Parity, Overrun and Framing**
- **Compatible with an Extended Range of Intel Microprocessors**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Available in EXPRESS and Military Versions**

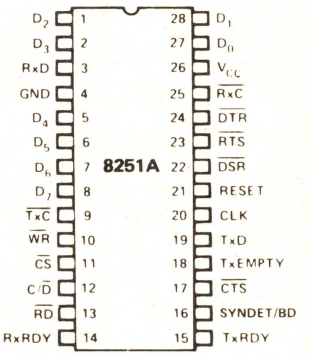
3

The Intel 8251A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using Intel's high performance HMOS technology.



205222-1

Figure 1. Block Diagram



205222-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 205222-003

82050
ASYNCHRONOUS COMMUNICATIONS CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 8-Bit Character Format**
  - **— Odd-, Even-, or No-Parity Generation and Detection**
  - **— Serial Bit Rate: DC to 56 Kb/s**
- **Programmable, 16-Bit Baud Rate Generator**
- **System Clock**
  - **— On-Chip Crystal Oscillator**
  - **— Externally Generated Clock**
- **28-Lead DIP and PLCC Packages**
- **IBM PC (INS 16450/8250A) Software Compatible**
- **Seven I/O Pins**
  - **— Dedicated Modem I/O**
  - **— General Purpose I/O**
- **No-TTL Interface to Most Intel Processors**
- **Internal Diagnostics with Local Loopback**
- **Complete Interrupt and Status Reporting**
- **CHMOS III Technology Provides Increased Reliability and Reduced Power Consumption**
- **Line Break Generation and Detection**

The Intel CHMOS 82050 Asynchronous Communications Controller is a low cost, higher performance alternative to the INS 16450—it emulates the INS 16450 and provides 100% compatibility with IBM PC software. Its 28-lead package provides all the functionality necessary for an IBM PC environment while substantially decreasing board space requirements. The 82050's simpler system interface reduces TTL glue—especially for higher frequency PC bus designs. The 82050 provides a low cost, high-performance integrated modem solution when combined with Intel's 89024 modem chip set. The compact 28-pin 82050 is fabricated using CHMOS III technology for decreased power consumption and increased reliability.

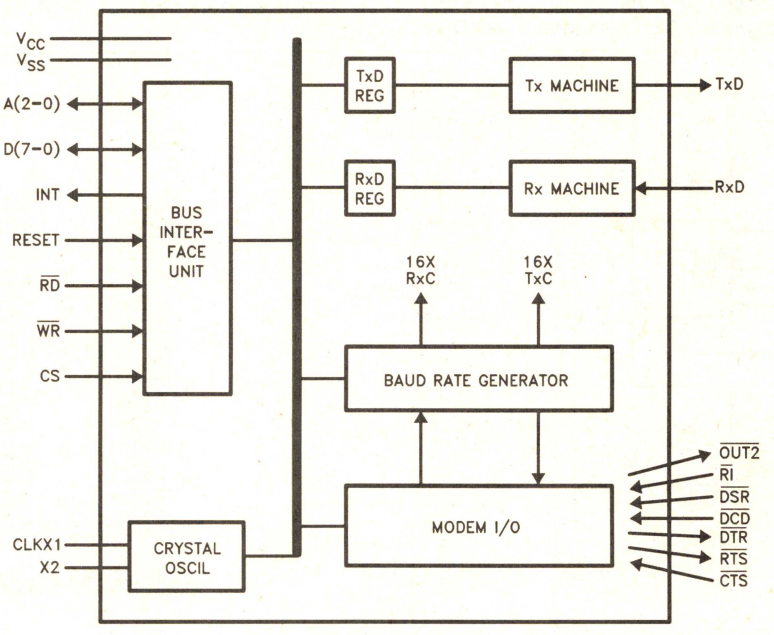


Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 290137-005

82510
ASYNCHRONOUS SERIAL CONTROLLER

- **Asynchronous Operation**
  - **— 5- to 9-Bit Character Format**
  - **— Baud Rate DC to 288k**
  - **— Complete Error Detection**
- **Multiple Sampling Windows**
- **Two, Independent, Four-Byte Transmit and Receive FIFOs with Programmable Threshold**
- **Two, 16-Bit Baud Rate Generators/ Timers**
- **System Clock Options**
  - **— On-Chip Crystal Oscillator**
  - **— External Clocks, Low/High Speed**
- **MCS-51 9-Bit Protocol Support**
- **IBM PC AT* (INS 8250A/16450) Software Compatible**
- **Control Character Recognition**
- **CHMOS III with Power Down Mode**
- **Interrupts Maskable at Two Levels**
- **Auto Echo and Loopback Modes**
- **Seven I/O Pins, Dedicated and General Purpose**
- **28-Lead DIP and PLCC Packages**

(See Packaging Spec., Order #: 231369)

The Intel CHMOS 82510 is designed to increase system efficiency in asynchronous environments such as modems or serial ports—including expanding performance areas: MCS-51 9-bit format and high speed async. The functional support provided in the 82510 is unparalleled—two baud rate generators/timers provide independent data rates or protocol timeouts; a crystal oscillator and smart modem I/O simplify system logic. New features, dual FIFOs and Control Character Recognition (CCR), dramatically reduce CPU interrupts and increase software efficiency. The 82510's software versatility allows emulation of the INS8250A/16450 for IBM PC AT* compatibility or a high-performance mode, configured by 35 control registers. All interrupts are maskable at two levels. The multipersonality I/O pins are configurable as desired. A DPLL and multiple sampling of serial data improve data reliability for high-speed, asynchronous communication. The compact 28-pin 82510 is fabricated with CHMOS III technology and includes a software powerdown option.

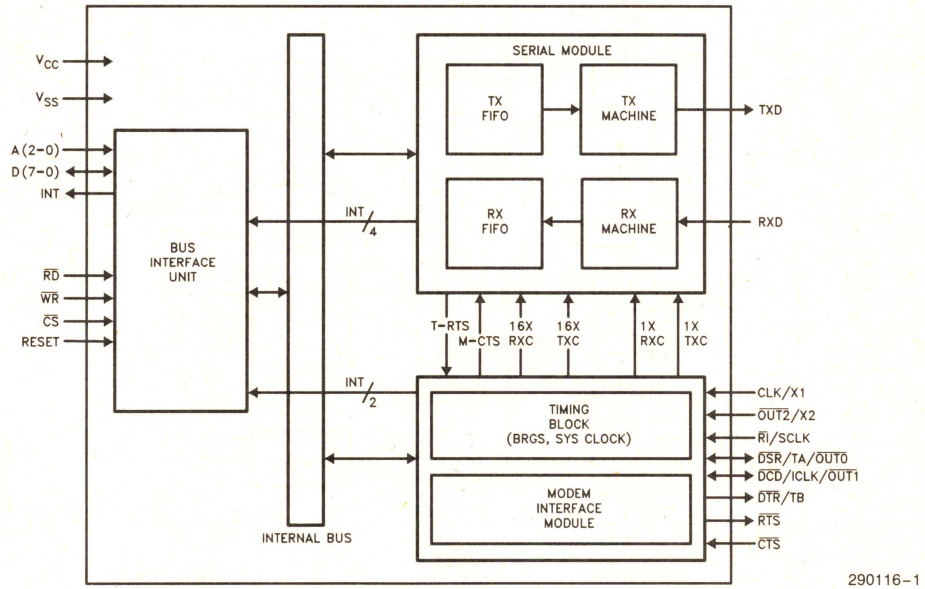


Figure 1. Block Diagram

*IBM and PC AT are trademarks of International Business Machines.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 290116-005

8273
PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

- CCITT X.25 Compatible
- HDLC/SDLC Compatible
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Up to 64K Baud Synchronous Transfers
- Automatic FCS (CRC) Generation and Checking
- Up to 9.6K Baud with On-Board Phase Locked Loop
- Programmable NRZI Encode/Decode
- Two Programmable Modem Control Ports
- Digital Phase Locked Loop Clock Recovery
- Minimum CPU Overhead
- Fully Compatible with 8048/8080/8085/8088/8086/80188/80186 CPUs
- Single +5V Supply

The Intel 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/CCITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS 188/186. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

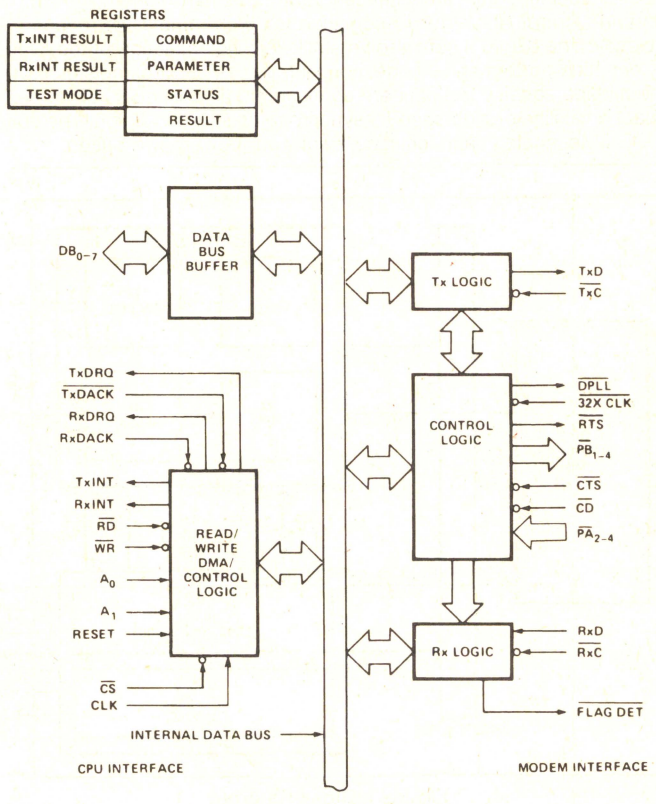


Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

December 1992
Order Number: 210479-004

8274
MULTI-PROTOCOL SERIAL CONTROLLER (MPSC)

- **Asynchronous, Byte Synchronous and Bit Synchronous Operation**
- **Two Independent Full Duplex Transmitters and Receivers**
- **Fully Compatible with 8048, 8051, 8085, 8088, 8086, 80188 and 80186 CPU's; 8257 and 8237 DMA Controllers; and 8089 I/O Proc.**
- **4 Independent DMA Channels**
- **Baud Rate: DC to 880K Baud**
- **Asynchronous:**
  - **— 5–8 Bit Character; Odd, Even, or No Parity; 1, 1.5 or 2 Stop Bits**
  - **— Error Detection: Framing, Overrun, and Parity**
- **Byte Synchronous:**
  - **— Character Synchronization, Int. or Ext.**
  - **— One or Two Sync Characters**
  - **— Automatic CRC Generation and Checking (CRC-16)**
  - **— IBM Bisync Compatible**
- **Bit Synchronous:**
  - **— SDLC/HDLC Flag Generation and Recognition**
  - **— 8 Bit Address Recognition**
  - **— Automatic Zero Bit Insertion and Deletion**
  - **— Automatic CRC Generation and Checking (CCITT-16)**
  - **— CCITT X.25 Compatible**
- **Available in EXPRESS and Military**

3

The Intel 8274 Multi-Protocol Series Controller (MPSC) is designed to interface High Speed Communications Lines using Asynchronous, IBM Bisync, and SDLC/HDLC protocol to Intel microcomputer systems. It can be interfaced with Intel's MCS-48, -85, -51; iAPX-86, -88, -186 and -188 families, the 8237 DMA Controller, or the 8089 I/O Processor in polled, interrupt driven, or DMA driven modes of operation.

The MPSC is a 40 pin device fabricated using Intel's High Performance HMOS Technology.

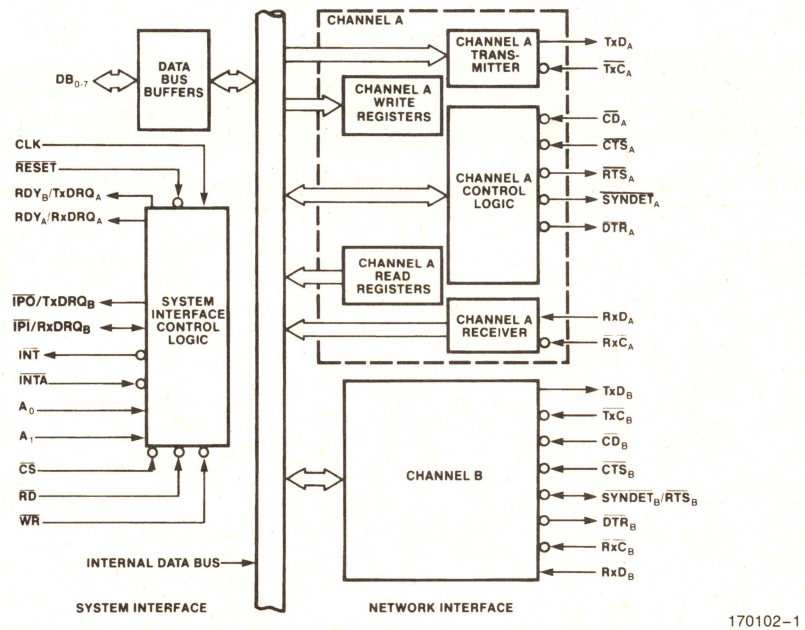


Figure 1. Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 170102-004

82530/82530-6
SERIAL COMMUNICATIONS CONTROLLER (SCC)

- **Two Independent Full Duplex Serial Channels**
- **On Chip Crystal Oscillator, Baud-Rate Generator and Digital Phase Locked Loop for Each Channel**
- **Programmable for NRZ, NRZI or FM Data Encoding/Decoding**
- **Diagnostic Local Loopback and Automatic Echo for Fault Detection and Isolation**
- **System Clock Rates:**
  - **— 4 MHz for 82530**
  - **— 6 MHz for 82530-6**
- **Max Bit Rate (6 MHz)**
  - **— Externally Clocked: 1.5 Mbps**
  - **Self-Clocked:**
  - **375 Kbps FM CODING**
  - **187 Kbps NRZI CODING**
  - **93 Kbps Asynchronous**
- **Interfaces with Any INTEL CPU, DMA or I/O Processor**
- **Available in 40 Pin DIP and 44 Lead PLCC**
- **Available in Express Version**
- **Asynchronous Modes**
  - **— 5–8 bit Character; Odd, Even or No Parity; 1, 1.5 or 2 Stop Bits**
  - **— Independent Transmit and Receive Clocks. 1X, 16X, 32X or 64X Programmable Sampling Rate**
  - **— Error Detection: Framing, Overrun and Parity**
  - **— Break Detection and Generation**
- **Bit Synchronous Modes**
  - **— SDLC Loop/Non-Loop Operation**
  - **— CRC-16 or CCITT Generation Detection**
  - **— Abort Generation and Detection**
  - **— I-field Residue Handling**
  - **— CCITT X.25 Compatible**
- **Byte Synchronous Modes**
  - **— Internal or External Character Synchronization (1 or 2 Characters)**
  - **— Automatic CRC Generation and Checking (CRC 16 or CCITT)**
  - **— IBM Bisync Compatible**

The INTEL 82530 Serial Communications Controller (SCC) is a dual-channel, multi-protocol data communications peripheral. It is designed to interface high speed communications lines using Asynchronous, Byte synchronous and Bit synchronous protocols to INTEL's microprocessors based systems. It can be interfaced with Intel's MCS51/96, iAPX86/88/186 and 188 in polled, interrupt driven or DMA driven modes of operation.

The SCC is a 40-pin device manufactured using INTEL's high-performance HMOS* II technology.

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* HMOS is a patented process of Intel Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

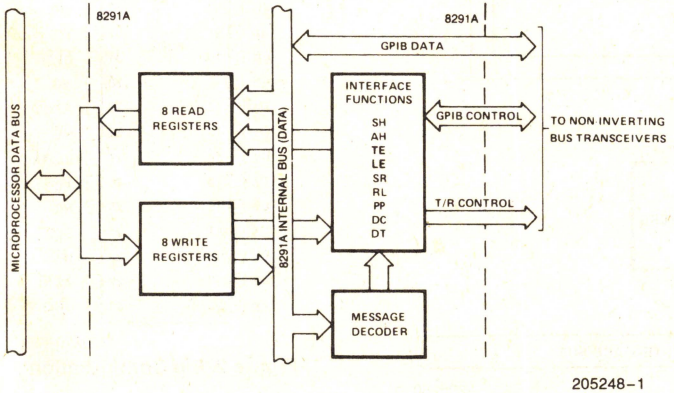
October 1987
Order Number: 230834-003

8291A
GPIB TALKER/LISTENER

- Designed to Interface Microprocessors (e.g., 8048/49, 8051, 8080/85, 8086/88) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1–8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Tranceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

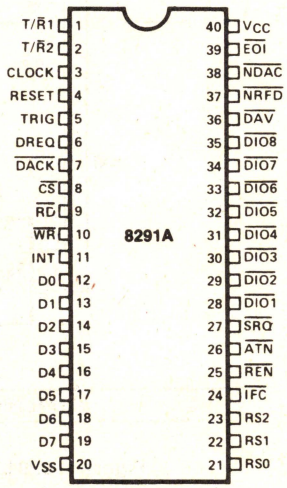
3

The 8291A is an enhanced version of the 8291 GPIB Talker/Listener designed to interface microprocessors to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller. The controller function can be added with the 8292 GPIB Controller.



205248-1

Figure 1. Block Diagram



205248-2

Figure 2. Pin Configuration

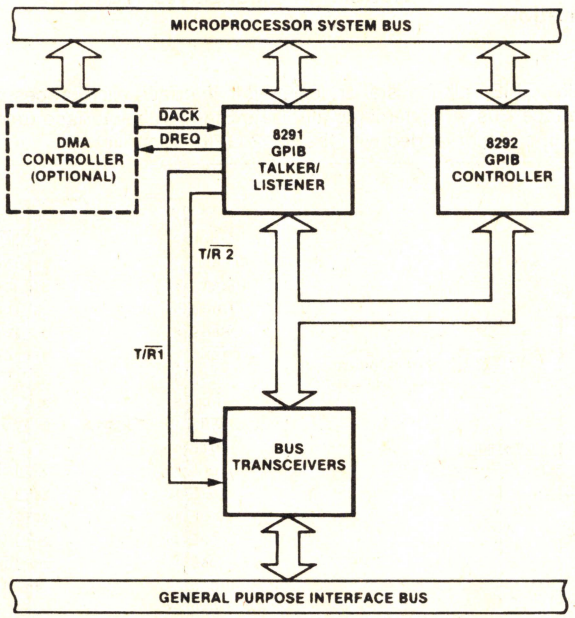
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 205248-003

8292
GPIB CONTROLLER

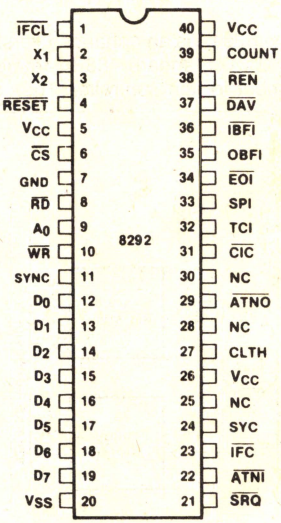
- **Complete IEEE Standard 488 Controller Function**
- **Interface Clear (IFC) Sending Capability Allows Seizure of Bus Control and/or Initialization of the Bus**
- **Responds to Service Requests (SRQ)**
- **Sends Remote Enable (REN), Allowing Instruments to Switch to Remote Control**
- **Complete Implementation of Transfer Control Protocol**
- **Synchronous Control Seizure Prevents the Destruction of Any Data Transmission in Progress**
- **Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller**

The 8292 GPIB Controller is a microprocessor-controlled chip designed to function with the 8291 GPIB Talker/Listener to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a preprogrammed Intel 8041A.



205250-1

Figure 1. 8291, 8292 Block Diagram



205250-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 205250-003

8294A
DATA ENCRYPTION/DECRYPTION UNIT

- **Certified by National Bureau of Standards**
- **400 Byte/Sec Data Conversion Rate**
- **64-Bit Data Encryption Using 56-Bit Key**
- **DMA Interface**
- **3 Interrupt Outputs to Aid in Loading and Unloading Data**
- **7-Bit User Output Port**
- **Single 5V ± 10% Power Supply**
- **Fully Compatible with iAPX-86, 88, MCS-85, MCS-80, MCS-51, and MCS-48 Processors**
- **Implements Federal Information Processing Data Encryption Standard**
- **Encrypt and Decrypt Modes Available**

The Intel 8294A Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294A; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294A in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 400 bytes/second. The 8294A also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294A implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

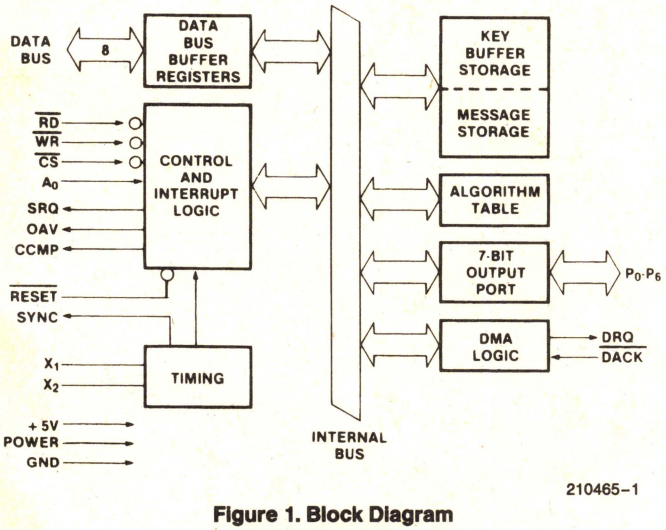


Figure 1. Block Diagram

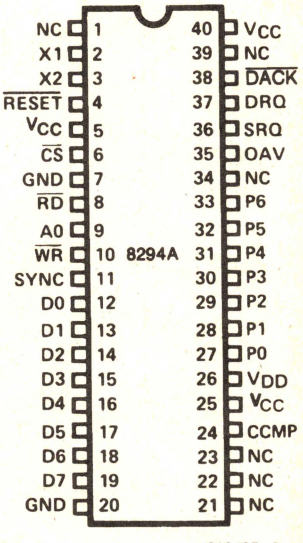


Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM system. To obtain a copy, contact your local Intel field sales office, Intel technical distributor or call 1-800-548-4725.

September 1993
Order Number: 210465-005

Appendix 4

APPENDIX A

ADDITIONAL TECHNICAL DOCUMENTATION

Document Title	Order Number:
Modem Hardware Reference Manual	296235-003
Modem Software Reference Manual	296503-002

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As a leading provider of connectivity solutions, Intel offers a wide range of products for desktop and mobile PC wide area connectivity and other telecommunications applications.

This handbook contains product data sheets, design and application information for Intel's entire line of connectivity products, including the 89C124FX Data Fax Modem Chip Set for desktop and notebook PCs. Also included in the handbook are application articles that explore Intel's Connectivity Product Line while the charts show parameters, test conditions and layout principles.

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